

White Paper

A Tale of Two Data Sheets and How Foil Roughness Affects Dk

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Abstract:

When doing stackup and impedance modeling, we need to get the dielectric material properties from the right sources. One important parameter for accurate impedance modeling is the dielectric constant or simply Dk. In this paper the difference between simple laminate suppliers' marketing data sheets and engineering data sheets are discussed as well as how foil roughness affects the effective Dk.

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A Tale of Two Data Sheets and How Foil Roughness Affects Dk

When doing printed circuit board (PCB) stackup and signal integrity (SI) impedance modeling, we need to get the dielectric material properties from the right sources. One important parameter for accurate impedance modeling is relative permittivity (ε_r) of the dielectric material, otherwise known as dielectric constant (Dk). The best source is from laminate suppliers' data sheets. But there is an issue I like to think of as, "A tale of two data sheets".

Marketing data sheets, like the example shown in Figure 1, are easily found on laminate suppliers' websites. They are meant for quick comparison of dielectric properties to narrow your search for the right laminate for your application. Dielectric properties on marketing data sheets include mostly thermal and mechanical properties, which are important for the physical structure of the material and how it will perform with other material properties in the stackup during processing.

But, marketing data sheets are not representative of what is needed to design an actual stackup, or to do impedance and SI loss modeling. Depending on glass style, resin content, thickness, Dk and dissipation factor (Df) will be different for different cores and prepreg thicknesses for the same laminate. Marketing data sheets usually only report a typical Dk/Df at fifty percent resin content and two or three frequency points. Thickness is not specified. Furthermore, Dk and Df are not constant over frequency. So using numbers from these data sheets, will lead to inaccurate impedance and phase delay results.

Typical Values Table

	Property	Typical Value	Units	Test Method	
		Metric (English)	IPC-TM-650 (or as noted)		
Glass Transition Temperature (Tg) by	DSC	200	°C	2.4.25C	
Glass Transition Temperature (Tg) by	220	°C	2.4.24.4		
Glass Transition Temperature (Tg) by	180	°C	2.4.24C		
Decomposition Temperature (Td) by	TGA @ 5% weight loss	360	°C	2.4.24.6	
Time to Delaminate by TMA	A. T260	>60	Minutes		
(Copper removed)	B. T288	>60		2.4.24.1	
	C. T300	>20			
7 Avia OTE	A. Pre-Tg	45	ppm/°C	24240	
Z-AXIS CTE	C. 50 to 260°C. (Total Expansion)	25	%	2.4.240	
X/Y-Axis CTF	Pre-Ta	15	ppm/°C	2 4 240	
Thermal Conductivity		0.42	W/m·K	ASTM F1952	
Thermal Stress 10 sec @ 288°C	A Unetched	0.12			
(550.4°F)	B. Etched	Pass	Pass Visual	2.4.13.1	
	A. @ 2 GHz	3.04		2.5.5.5	
Dk, Permittivity	B. @ 5 GHz	3.02	-		
	C. @ 10 GHz	3.02			
	A. @ 2 GHz		-	2.5.5.5	
DT, Loss Tangent		0.0021			
Volume Resistivity	C-96/35/90		Mil-cm	2 5 17 1	
Surface Resistivity	C-96/35/90	1.33x10 ⁵	M	2.5.17.1	
Dielectric Breakdown	60	kV	2.5.6B		
Arc Resistance		125	Seconds	2.5.1B	
Electric Strength (Laminate & laminat	ed prepreg)	60 (1500)	kV/mm (V/mil)	2.5.6.2A	
				UL 746A	
Comparative Tracking Index (CTI)	3	Class (Volts)	ASTM D3638		
	A. Low profile copper foil and very low profile copper foil	0.79 (4.5)	N/mm (lb/inch)	2480	
Peel Strength	all copper foil >17 Im [0.669 mil]			2.4.00	
	B. Standard profile copper 1. After thermal stress	0.96 (5.5)		2.4.8.2A	
	A. Length direction	44.0			
Flexural Strength	B. Cross direction	41.0	KSI	2.4.4B	
Tensile Strength	A. Length direction	30.0	kei	ASTM D3039	
	B. Cross direction	25.0	Kai	ASTM D2028	
Young's Modulus	A. Length direction	2,551 2,417	ksi	ASTM D790-15e2	
	B. Cross direction				
Taylor's Modulus	A. Length direction B. Cross direction	2,264	ksi	ASTM D790-15e2	
	A. Length direction	0.165			
Poisson's Ratio	B. Cross direction	0.156	-	ASTM D3039	
Moisture Absorption	0.1	%	2.6.2.1A		
Flammability (Laminate & laminated p	Flammability (Laminate & laminated prepreg)			UL 94	
Relative Thermal Index (RTI)	130	°C	UL 796		

Figure 1 Example of a "Marketing" data sheet easily obtained from laminate supplier's web site. Source Isola Group [6].

Instead, for transmission line modeling, one needs to use the same Dk/Df table data sheets PCB fabricators use to build the stackup. An example Dk/Df table is shown in Figure 2. Dk/Df tables provide the actual core and prepreg thicknesses, resin content and Dk/Df, for the different glass styles, over different frequencies. Depending on the stackup, a combination of thicknesses are often needed to meet impedance requirements. Each thickness will have a different Dk value.

Prepreg Dielectric Constant(Dk) / Dissipation factor (Df) Table

Prepreg Data

Class Style	Resin	Offering	Thickness (inch)	Thickness (mm)	Dielectric Constant (DK)/ Dissipation Factor (DF)					
Class Style Co	Content %				1 GHz	2 Ghz	5 Ghz	10 GHz	15 Ghz	20 Ghz
1035	69.0%	Standard	0.0020	0.051	3.06 0.0017	3.06 0.0017	3.06 0.0017	3.06 0.0017	3.06 0.0017	3.06 0.0017
1067	70.0%	Standard	0.0022	0.056	3.05 0.0017	3.05 0.0017	3.05 0.0017	3.05 0.0017	3.05 0.0017	3.05 0.0017
106	76.0%	Standard	0.0023	0.058	2.95 0.0013	2.95 0.0013	2.95 0.0014	2.95 0.0014	2.95 0.0014	2.95 0.0014
1067	71.5%	Standard	0.0024	0.061	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.02 0.0016
1035	75.0%	Standard	0.0026	0.066	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014
1067	74.0%	Standard	0.0026	0.066	2.98 0.0014	2.98 0.0014	2.98 0.0015	2.98 0.0015	2.98 0.0015	2.98 0.0015
1067	76.5%	Standard	0.0029	0.074	2.94 0.0013	2.94 0.0013	2.94 0.0013	2.94 0.0013	2.94 0.0013	2.94 0.0013
1078	65.0%	Standard	0.0029	0.074	3.14 0.0019	3.14 0.0019	3.14 0.0019	3.14 0.0019	3.14 0.0019	3.14 0.0019
1078	67.5%	Standard	0.0031	0.079	3.09 0.0018	3.09 0.0018	3.09 0.0018	3.09 0.0018	3.09 0.0018	3.09 0.0018
1078	70.5%	Standard	0.0035	0.089	3.04 0.0016	3.04 0.0016	3.04 0.0016	3.04 0.0016	3.04 0.0016	3.04 0.0016
1080	72.0%	Standard	0.0038	0.097	3.02 0.0015	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.01 0.0016
1078	72.0%	Standard	0.0037	0.094	3.02 0.0015	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.02 0.0016	3.01 0.0016
1078	75.0%	Standard	0.0042	0.107	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014
1080	75.0%	Standard	0.0043	0.109	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014	2.97 0.0014
1080	78.0%	Alternate	0.0046	0.117	2.92 0.0013	2.92 0.0013	2.92 0.0014	2.92 0.0014	2.92 0.0014	2.92 0.0014
1078	78.0%	Alternate	0.0046	0.117	2.92 0.0013	2.92 0.0013	2.92 0.0014	2.92 0.0014	2.92 0.0014	2.92 0.0014
3313	63.5%	Standard	0.0046	0.117	3.16 0.0020	3.16 0.0020	3.16 0.0020	3.16 0.0020	3.16 0.0020	3.16 0.0020
3313	66.5%	Standard	0.0051	0.129	3.11 0.0018	3.11 0.0018	3.11 0.0018	3.11 0.0018	3.11 0.0018	3.11 0.0018
2116	62.0%	Standard	0.0058	0.147	3.19 0.0021	3.19 0.0021	3.19 0.0021	3.19 0.0021	3.19 0.0021	3.19 0.0021

Figure 2 Example of a typical "Engineering" data sheet showing Dk/Df table for different glass styles and resin content over frequency. Source Isola Group [6].

Many engineers assume Dk published is the intrinsic property of the material. But in fact, it is the effective Dk (Dkeff) measured by a specific industry standard test method. When they are compared against real measurements from a design application, there is often a discrepancy in Dkeff, due to increased phase delay caused by surface roughness [1].

Dkeff is highly dependent on the test apparatus and conditions of how it is measured. One method commonly used by many laminate suppliers is the clamped stripline resonator test method, as described by IPC-TM-650 2.5.5, Rev C, Test Methods Manual [11].

Since all glass reinforced laminates are anisotropic, any stripline based test method, like TM-650 2.5.5.5, or Bereskin stripline test method [16], reports Dk values in which the E-fields are transverse to signal propagation. I.E., if the signal propagation is in the x-y axis direction, then the Dk measured by this method is when E-fields are in the z-axis direction.

For Isola's Dk/Df table, shown in Figure 2, Dk values were measured by TM-650 2.5.5.5 test method. From that data, the values for most of the constructions are calculated. Additional verification runs are performed to gather statistical data over time and validate the calculations are reasonable and accurate.

The measurements are done under stripline conditions using a carefully designed resonant element pattern card. It is made with the same dielectric material to be tested. As shown in Figure 3, the card is sandwiched between two sheets of uncladded dielectric material under test. Then the whole structure is clamped between two large plates; each lined with copper foil and are grounded. They act as reference planes for the stripline.



Side View (Clamped) N.T.S.



This test method assures consistency of product when used in fabricated boards. It <u>does not</u> <u>guarantee</u> the values directly correspond to design applications.

Here's why:

Since the resonant element pattern card and material under test are not physically bonded together, air is entrapped between the various layers. These small air gaps are caused by;

- the roughness of the copper foil plates in the fixture
- the roughness profile imprint left on the surface from the foil that was removed from the test samples
- the copper removed on the resonant element pattern card

Air entrapment, due to TM-650 test method, is the primary reason for effective Dk and phase delay discrepancies between simulation using laminate suppliers' Dk/Df tables and real measurements from a design application. The small air gaps result in a lower effective Dk than what would be measured in a real PCB because everything is pressed together with no air entrapment, as shown in a cross-section view of Figure 4.



Figure 4 Example of foil bonded to core or prepreg dielectric. Rz_1 is rougher than Rz_2 and H_{smooth} is the thickness of the dielectric as if the foil was removed.

When copper roughness is different on each side of the dielectric, like the example shown in Figure 4, Dkeff is determined heuristically by this simple correction factor:

Equation 1

$$Dkeff \approx \frac{H_{smooth}}{\left(H_{smooth} - \left(Rz_1 + Rz_2\right)\right)} \times Dk$$

where:

• H_{smooth} is dielectric core thickness from laminate suppliers' Dk/Df table data sheet or pressed prepreg thickness from the PCB stackup drawing.

- Rz₁ and Rz₂ are the conductor roughness of the foil for the respective side of the dielectric from foil suppliers' data sheet. Typically Rz is the 10-point mean roughness as measured by a mechanical profilometer.
- Dk is dielectric constant from laminate supplier's Dk/Df table data sheet.

In Figure 4, Rz_1 is the roughness of the top foil and Rz_2 is the roughness of the bottom foil. In this example Rz_1 is rougher than Rz_2 . H_{smooth} is the core thickness of the dielectric, as specified in the Dk/Df table, or pressed thickness of the prepreg, shown on a stackup drawing. It is the thickness of the dielectric as if the foil was removed.

When copper foil with the same Rz roughness is bonded to each side of the core or prepeg, Dkeff can be simplified as:

Equation 2

$$Dkeff \approx \frac{H_{smooth}}{(H_{smooth} - 2Rz)} \times Dk$$

Figure 5 plots Dkeff over frequency derived from S21 phase or time delay (TD); $Dkeff = (TDc_0 / length)^2$ from a Megtron-6 stripline case study [3]. This method is different than IPC-TM-650 test method in that it determines Dkeff from unwrapped phase delay rather than calculating Dk/Df from resonant peaks over the frequency range defined in the spec.

The blue plot is a simulated case based on core and prepreg Dk values from published Dk/Df tables at 12GHz. When Dk is corrected, due to roughness using Equation 2 and resimulated, Dkeff is shown in pink. Although the Dkeff has improved, it still does not agree with the measured Dkeff from the device under test (DUT), shown in red.



Figure 5 Comparisons of simulated Dkeff over frequency vs measured. The red plot is actual measured Dkeff from the DUT. The middle pink plot is a simulation using Dkeff corrected due to roughness. The bottom blue plot is simulated using Dk @12GHz as published in Dk/Df tables and non-causal roughness model. The green dashed plot is a simulation using Dkeff due to roughness and a causal Huray-Bracken roughness model was used. Modeled with Simbeor [12] and simulated with Keysight ADS [13].

The discrepancy between the pink and red plots is because Dkeff from Equation 2, only corrects the phase delay due to self capacitance (C_{11}) per unit length of the transmission line. But roughness of the foil also increases the self inductance (L_{11}) per unit length of the transmission line, which adds additional phase or time delay [4].

This is counter intuitive and can be confusing since we usually relate Dkeff to capacitance only. By definition, Dkeff is the ratio of the actual structure's capacitance to the capacitance when the dielectric is replaced by air. But this is only true for static electric fields. For time-variant electromagnetic fields, Dkeff becomes frequency-dependent [15].

If the propagation delay (*tpd*) for a single transmission line, in seconds per unit length, is determined by:

Equation 3

$$tpd = \frac{\sqrt{\varepsilon_r}}{c_0} = \frac{\sqrt{Dkeff}}{c_0} = \sqrt{L_{11}C_{11}}$$

and; c_0 is the speed of light (~3.0E8 m/s) = $(\sqrt{\mu_0 \varepsilon_0})^{-1}$; μ_0 (4 π E-7 H/m) and ε_0 (8.8542E-12 F/m) is permeability and permittivity of free space respectively;

then:

Equation 4

$$Dkeff = \frac{L_{11}C_{11}}{\mu_0 \varepsilon_0}$$

Where: L_{11} ; C_{11} are self inductance in Henries per unit length and self capacitance in Farads per unit length respectively.

Equation 4 clearly shows that with an increase in self inductance there will be a proportional increase in Dkeff. This means for lossy PCB transmission lines, calculating $Dkeff = (TDc_0 / length)^2$ cannot be trusted to be the same as relative permittivity (ε_r) of the dielectric material. The consequence for doing so leads to inaccurate impedance predictions and non-causal time domain simulations, resulting in poor correlation to measurements.

A causal model, when simulated, does not produce any change in its output signal before there is a change in its input signal. When field solvers properly correct the self inductance, by applying the roughness correction factor to the imaginary portion of the complex impedance of the metal [4][5], the model is then causal. When combined with the corrected Dkeff for cores and prepregs from Equation 2, there is excellent correlation; as shown by the dashed green plot in Figure 5. Unfortunately, not all field solvers have causal roughness models to correct the inductance in the simulation.

Since there is no simple way to backtrack from a phase measurement to establish the right Dkeff to use for your modeling, especially for lossy stripline constructions, heuristic methods are an alternative.

Using the right Dkeff for your modeling ensures correct time domain reflectometer (TDR) impedance prediction, as shown in Figure 6. The red plot is measured differential TDR from [3]. When core and prepreg Dk from Dk/Df tables were used along with a non-causal roughness model in the simulation, the blue plot shows an over estimate for impedance. When Dkeff from Equation 2 and a non-causal roughness model was used in the simulation, the pink plot shows an underestimate in the impedance plot.

But it's only when we apply a causal Huray-Bracken roughness model from [12], along with Dkeff from Equation 2, we see the effect of the increased self inductance, shown by the green dashed line plot in Figure 6.

At first glance of Figure 6, one might interpret the pink plot has having better correlation to the measured red plot. But because the measured plot has an impedance ripple along its length, it is difficult to conclude which is the correct model from the TDR plots alone. It's only when we compare Dkeff derived from green dashed phase delay plot from Figure 5, we can conclude the green dashed line TDR plot is the correct impedance.



Differential TDR

Figure 6 Simulated vs measured differential TDR plots when different Dkeff was used in the model. The blue plot over estimates impedance when Dk from data sheets was used. The pink plot under estimates the impedance when Dkeff (Equation 2) and non-causal roughness model was used. The green dashed line plot is with Dkeff (Equation 2) and a causal Huray-Bracken roughness model was used. Modeled with Simbeor [12] and simulated with Keysight ADS [13].

Rogers Corporation [7] understand this. That's why they provide the "design" Dk in addition to their bulk Dk, as measured by TM650. The design Dk is an average number using a differential phase length method from several different tested lots of material and on the most common thickness.

This method is based on measuring phase difference from two identical microstrip transmission line geometries of different lengths on the same panel. Because this is a real microstrip application, the dielectric is fully bonded to the copper and there is no air entrapment. Knowing the phase and length difference, the effective Dk can be easily determined .

The accuracy of the resultant effective Dk depends on several factors like:

- fixture design
- length ratio between two transmission lines
- material thickness of the sample under test

- the thickness of the copper
- actual roughness of the foil on the microstrip circuit.

In lieu of actual Dk/Df tables, Rogers provide a handy impedance calculator as shown in in the RO4003C example of Figure 7. There are three Dk options available to use:

- Z-axis Bulk Dk
- Dk values for specific frequencies
- Dk values for characteristic impedance

The first radio button, as shown in Figure 7, gives the z-axis bulk Dk value of 3.55, as measured by TM650 2.5.5.5 test method manual. However, the value does not change when different frequencies are selected. This makes the number suspect since clearly design Dk does change over frequency. Thus this number can be considered equivalent to marketing data sheets, and should not be used.

When the middle radio button is selected, a Dk value for a specific frequency is displayed, which corresponds to a frequency entered in the lower right frequency box of Figure 7. This is the most useful option, since it allows the user to choose the right design Dk at whatever frequency they choose for their application, including characteristic impedance. This option factors in the foil roughness effect, so no correction factor is needed to use in your simulator.

The last radio button selects a *Dk for characteristic impedance* calculation. It is a "design" Dk with yet a different Dk. Similar to the *Bulk Dk* option, it does not change over frequency. For any simulation tool other than the Rogers's calculator, *Bulk Dk* and *Dk values for characteristic impedance* values should not be used.



Figure 7 Example of Rogers Corporation impedance calculator. For an 8-mil thick RO4003C dielectric, bulk Dk is 3.55 while design Dk over frequency is shown in bottom left window.

Under the information tab, the user can download design Dk over frequency, for a specified thickness, shown in the bottom left window of Figure 7. This data can be selected and copied to the clipboard and pasted into a spreadsheet for further processing.

Figure 8 plots design Dk vs frequency for various thickness from 8 mils to 60 mils for RO4003C material. As can be seen, design Dk is not constant over frequency and furthermore it is different for different thicknesses, mainly due to the roughness of the foil that is already included in the measurement.

Thinner material has a higher design Dk than thicker material, for the same roughness of foil. This is because when the foil teeth protrude into a thin dielectric material, there is a higher concentration of e-fields, resulting in higher capacitance between top and bottom copper layers. For thick dielectrics the foil teeth have less of an impact on capacitance and thus Dkeff, as described mathematically by Equation 2.

Since the roughness of the foil does not significantly influence the design Dk for thick laminates, we can assume the bulk Dk is roughly equivalent to design Dk over frequency for the 60-mil laminate.



Figure 8 Design Dk vs frequency for various thickness of RO4003C from 8 mils to 60 mils mainly due to the roughness of the foil. Thinner material has a higher design Dk than thicker material, for the same roughness of foil.

Heuristically, we can rearrange Equation 2 and estimate the Rz roughness of the foil used on RO4003C laminate to be $6.302 \,\mu m$ from Equation 5.

Equation 5

$$Rz \approx 0.5 \left(H_{smooth} - \frac{H_{smooth} \times Dk_{Bulk}}{Dkeff} \right) \approx 0.5 \times \left(203 - \frac{203 \times 3.55}{3.785} \right) \approx 6.302 \,\mu m$$

where:

 H_{smooth} is the thickness of the 8 mil (203 μ m) laminate

 $Dk_{Bulk} = 3.55$ at 60 GHz

 $Dkeff = \text{design Dk of 8 mil (203 } \mu\text{m})$ laminate at 60 GHz

A cross-section sample from a TDR demo board, courtesy of Picotest [10], was measured and is shown in Figure 9. The TDR demo board was fabricated with 8-mil thick Rogers RO4003C core laminate and cladded with 2 Oz copper foil.

Five highlighted random sample lengths of copper roughness, labeled Sample 1 to Sample 5 of Figure 9, were analyzed. The total length of each respective sample was then equally partitioned into five equal sections, similar to the blow-up picture of Sample 1, to measure the maximum peak to valley height of each section. The five measurements of each sample length were then averaged to determine the Rz roughness, as described under IPC TM650 2.2.17A and shown in the table of Figure 9.

The mean value of Rz for the 5 samples was 6.176 μ m with a standard deviation (SD) of 1.090 μ m. This compares favorably with the estimated roughness of 6.302 μ m, determined from Equation 5.



Figure 9 A cross-section sample from a Rogers RO4003C based TDR demo board, courtesy of Picotest [10], used to determine Rz roughness of the foil.

When we use the actual roughness measured from Figure 9 and Equation 2, we can then calculate Dkeff at 60 GHz for different thicknesses, shown in Table 1. As can be seen there is, less than 1% delta compared with design Dk reported from the calculator!

Height mil	Height µm	Bulk Dk @ 60 GHz	Design Dk @ 60 GHz	Rz μm	Dkeff @ 60GHz	Delta
8.0	203	3.550	3.785	6.176	3.780	-0.13%
12.0	304	3.550	3.702	6.176	3.700	-0.04%
16.0	406	3.550	3.657	6.176	3.661	0.12%
20.0	508	3.550	3.625	6.176	3.638	0.37%
32.0	812	3.550	3.580	6.176	3.605	0.69%
60.0	1524	3.550	3.550	6.176	3.579	0.82%

Table 1 Comparison of Roger's Design Dk vs Dkeff when simple correction factor applied to BulkDk at 60 GHz.

Summary:

Dielectric constants from marketing data sheets cannot be trusted to properly design PCB stackups and model transmission lines for impedance and phase delay. Instead laminate suppliers' Dk/Df tables should be used.

Most laminate suppliers provide Dk/Df tables per a particular test method. But the numbers do not factor the actual roughness of the foil. When a simple correction factor, based on the thickness of laminate and Rz foil roughness is considered, a more accurate value for Dk can be used for impedance and transmission line modeling.

For PCB transmission lines is calculating Dkeff from phase or time delay measurement cannot be trusted to be the relative permittivity of the dielectric material. Using this value will lead to inaccurate simulation results.

Rogers Corporation provide a handy calculator in lieu of Dk/Df tables in which "design" Dk values over frequency can be used directly without correcting for roughness. When an actual cross-section was analyzed, there was excellent correlation from corrected Dkeff using heuristic methods compared to design Dk from the calculator. Therefore, "design" Dk should be used for impedance modeling and PCB stackup design.

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