EDI CON 2017 Electronic Design Innovation Conference & Exhibition
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Practical Modeling of High-speed Channels Based on Data Sheet Input

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***"When designing high-speed serial links above 10 GB/s, everything matters…."* – Dave Dunham, Molex**

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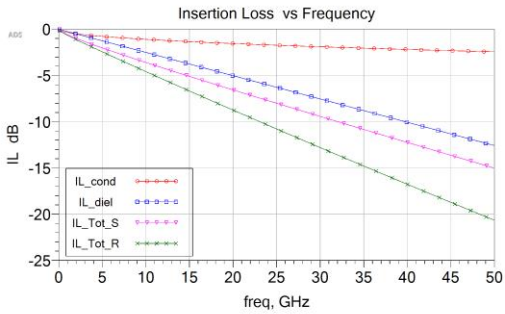
As Dave Dunham from Molex Corp. likes to say, "*When designing high-speed serial links beyond 10 GB/s, everything matters*".

Transmission Line Modeling



Important to model dielectric and conductor loss accurately

$$IL_{total}(f) = IL_{diel}(f) + K_{SR}(f) \times IL_{conductor}(f)$$

Simulated with Keysight ADS [12]

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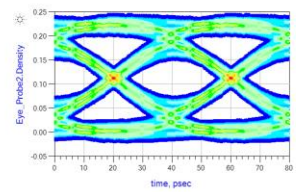
And part of that everything is accurate modeling of transmission line losses. It is important to model dielectric and conductor loss accurately. In this plot we see an example of a simulated transmission line with and without conductor roughness. Starting at the top, the red curve is the conductor loss without roughness. The next one down in blue is the dielectric loss. The pink curve is the sum of the dielectric and conductor loss without roughness, and finally the last curve in green is the total loss with conductor roughness.

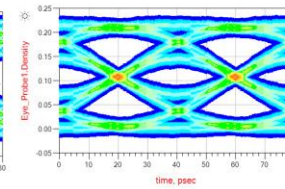
Failure To Model Roughness Properly Can Ruin You Day!

With just 3.2dB delta @12.5 GHz => ½ the eye height with rough copper

Smooth Copper



Rough Copper

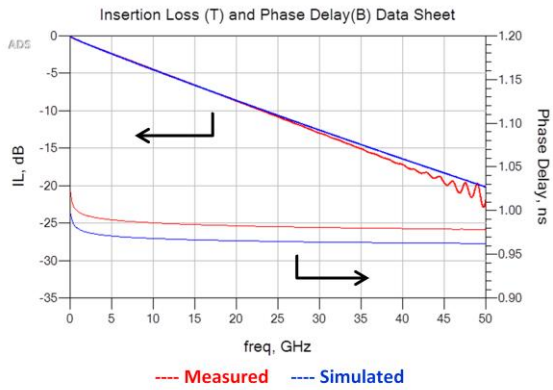


25Gb/s

Simulated with Keysight ADS [12]

Failure to account for conductor roughness can ruin you day especially if you are trying to push 25 GB/s NRZ signaling down your channel. As shown with just 3.2 dB delta in insertion loss, at 12.5 GHz Nyquist frequency, results in ½ the eye height when conductor roughness is taken into account.

Dielectric Properties



Failure to correct D_k from data sheet due to conductor roughness => inaccuracy in simulated IL & Phase Delay

Simulated with Keysight ADS [12]

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On top of that, failure to correct D_k from data sheet due to conductor roughness can lead to inaccuracy in simulated insertion loss (IL) & phase delay.

EDA Tool Challenges

✓ **Many EDA tools include latest and greatest models for conductor surface roughness and wideband dielectric properties**

But obtaining the right parameters to feed models is always a challenge

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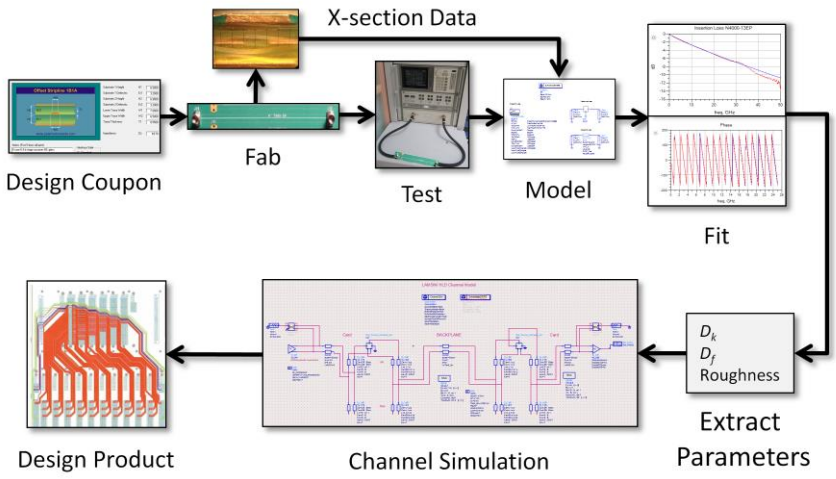
Many electronic design automation (EDA) tools include the latest and greatest models for conductor surface roughness and wide-band dielectric properties. But obtaining the right parameters to feed the models is always a challenge.

So how do we get these parameters?

Design Feedback Method



Benefits:

- Practical
- Accurate

Issues:

- Expertise Required
- Time
- Money

One way is to follow the design feedback method which involves designing, building and measuring a test coupon. After modeling and tuning various parameters to best fit measured data, D_k, D_f and roughness parameters can be extracted. They are then used in channel modeling software to design the final product.

***"Sometimes an OK answer NOW! is better than a good answer late…."* – Eric Bogatin**

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But, as my friend Eric Bogatin often likes to say, *"Sometimes an OK answer NOW! is better than a good answer late."* As a high-speed signal integrity practitioner and backplane architect, I often have to come up with an answer sooner, rather than later because of the impact to time and cost to my clients. And that's why I have been motivated over the last few years to research and develop a simple methodology to accurately determine parameters to feed into modern EDA tools.

What You Will Learn

- ✓How to use my Cannonball model to determine Huray roughness parameters from data sheet alone
- ✓How to determine D_{keff} due to roughness from data sheets alone
- ✓How to apply these parameters in the latest version of Polar Si9000e Field Solver
- ✓How to pull it all together using Keysight ADS software

Outline

- Modeling Conductor Roughness:
  - Overview
  - Hammerstad Model
  - Huray Model
  - Cannonball-Huray Model
- D_{keff} Due to Roughness Model
- Model Validation: CMP28 Platform / Polar Instruments Si9000e
- Example of Best Practice to Model High-speed Channels Based on Data Sheet Input: Amphenol-FCI ExaMax Backplane Reference Platform

Modeling Conductor Roughness

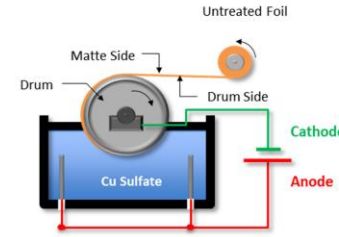
Copper Foil Manufacturing Processes

Rolled

- Smoother
- Higher Cost

VS

Electro-deposited (ED)



- Rougher
- Lower Cost

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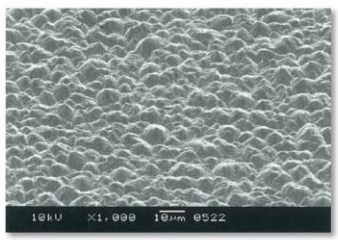
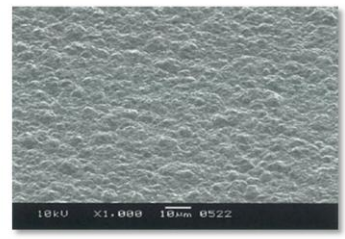
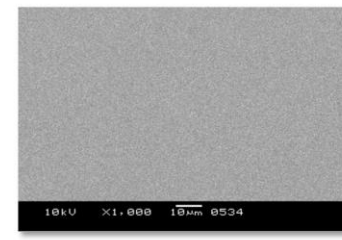
There are basically two kinds of copper foils used in the PCB world. They are rolled and electro-deposited copper foils. Rolled copper will always be smoother than ED copper, but is higher cost. ED copper is rougher and is most popular because of the lower cost.

It is important to note that ED copper has two sides to the foil. The matte side is the side facing the Cu sulphate solution. The drum side is the side facing the drum. The matte side is always rougher than the drum side.

Common Roughness Profiles

IPC Standard Profile	IPC Very Low Profile(VLP)	Ultra Low Profile (ULP)Class
		
No min/max spec	< 5.2 μm max	*-Other names: HVLP*, VSP -No IPC spec -Typically < 2 μm max

SEM Photos Reference [16]

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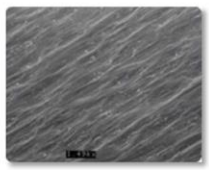
Here are three common foil roughnesses used in the PCB industry today. The most common is standard profile on the left. It has no min or maximum IPC roughness spec.

Very low profile roughness, in the center, is typically any foil with a roughness of less than 5.2 microns.

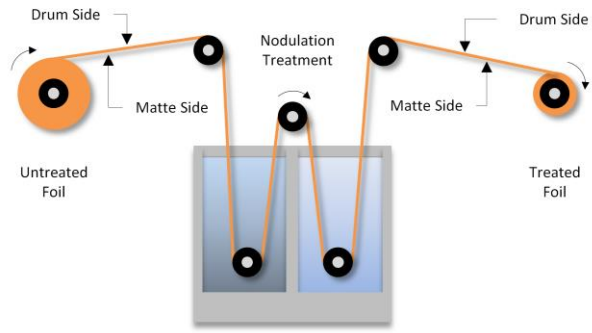
Ultra Low profile copper, on the right, is a newer class of copper with roughness less than 2 microns max. There is no official IPC spec as yet, so you will see proprietary names like HVLP, ULP, VSP.

Electro-deposited Copper Foil Nodulation Treatment

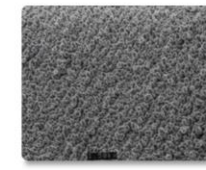


Drum Side Untreated

Matte Side Untreated

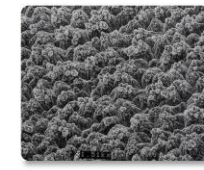


SEM Photos Courtesy [2]



Drum Side Treated

OR



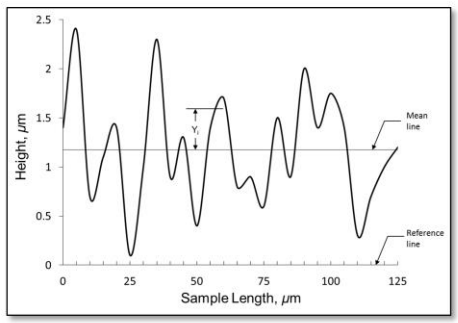
Matte Side Treated

Foil nodulation treatment is applied to either the matte side or drum side of the foil. On the left are SEM pictures of the untreated drum and matte sides as they come off the electrodeposited process.

After going through the nodulation treatment, tiny nodules are deposited on one side of the foil as shown by the SEM photos on the right. Normally nodules are applied to the matte side, but it is becoming more common for nodule treatment on the drum side. This is referred to as reverse-treated foil or RTF. Double side treated foil is available but is not that common.

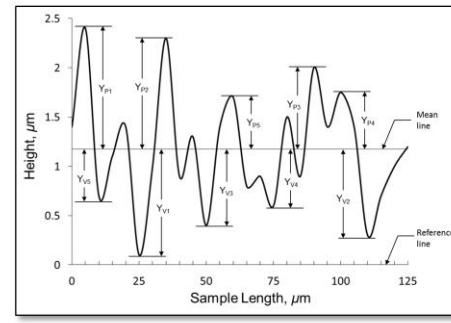
Roughness Parameters

RMS (R_q) / Average (R_a)



$$R_q = \sqrt{\frac{1}{N}\sum_{i=1}^{N} Y_i^2} \qquad R_a = \frac{1}{N}\sum_{i=1}^{N}|Y_i|$$

10-point Mean (R_z)



$$R_z = \frac{1}{5}\sum_{i=1}^{5}|Y_{Pi}| + \frac{1}{5}\sum_{i=1}^{5}|Y_{Vi}|$$

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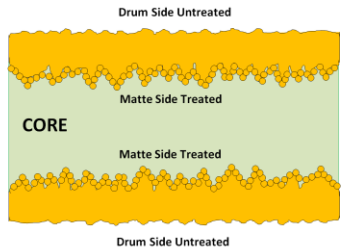
Typical tooth profile parameters reported in data sheets. The10-point mean parameter (*Rz*), is the most common for the matte and drum side. It is the sum of the average of the five highest peaks and the five lowest valleys of the rough conductor surface over the sample length.

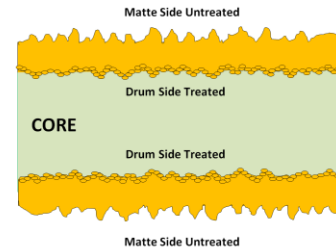
Sometimes average roughness (*Ra*) is reported for the drum side. And RMS roughness (*Rq*) may or may not be reported.

Foil Bonding to Core

Standard Treated Foil



Reverse Treated Foil (RTF)



✓ **Treated Side of Raw Foil Always Bonds to Core**

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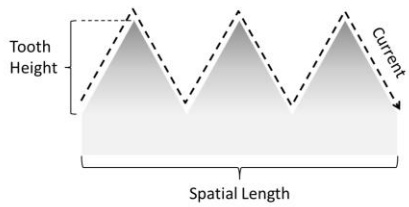
Here we see an example of how standard treated foil and reverse treated foil is bonded to core. The standard treated foil example sees the treated matte side bonded to the core, while reverse treated foil sees the treated drum side bonded to the core.

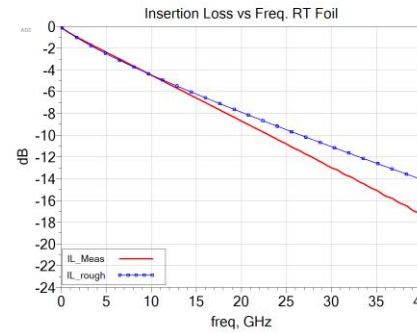
The important take away is that the nodule treated side is the one always bonded to the core laminate material, and is important to keep that in mind when you are modeling the channel.

Hamerstad & Jenson Model



$$K_{HJ} = \frac{P_{rough}}{P_{flat}} = 1 + \frac{2}{\pi}\arctan\left(1.4\left(\frac{\Delta}{\delta}\right)^2\right)$$

Δ = RMS tooth height in meters



Loses accuracy above ~ 3-15GHz depending on roughness of copper

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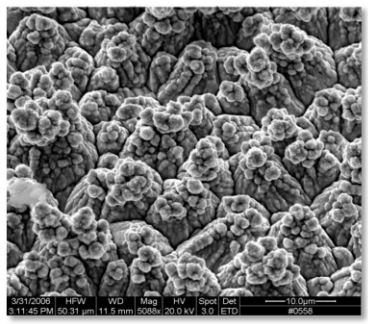
The Hammerstad model has been used for decades to model conductor roughness, since all that was required was the RMS value of the peak to valley roughness parameter from data sheets. But it loses accuracy after 3-15 GHz, depending on the roughness of copper foil.

Huray "*snowball*" Model [5]



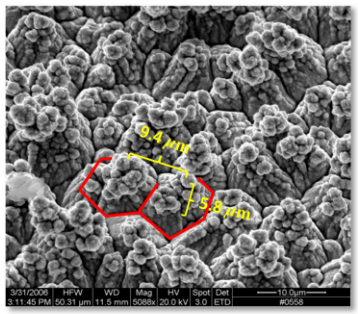
SEM Photo Reference [14]

Based on non-uniform distribution of spheres resembling "snowballs" applied to a matte base

$$K_{SRH}(f) = \frac{P_{rough}}{P_{flat}} \approx \frac{A_{matte}}{A_{flat}} + \frac{3}{2}\sum_{i=1}^{j}\left(\frac{N_i \times 4\pi a_i^2}{A_{flat}}\right)\left(1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2}\right)^{-1}$$

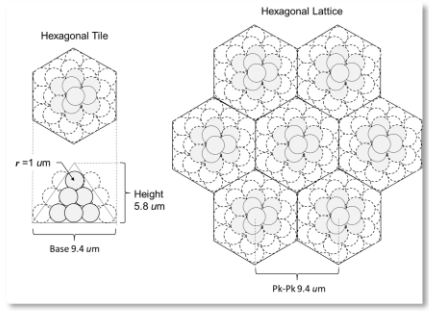
The Huray model has gained popularity over the last few years. It is based on non-uniform distribution of spheres resembling "snowballs" applied to a matte base. Although it is quite accurate, it is always difficult to obtain the right parameters for number of spheres, sphere radius and tile base area.

Huray Model Prior Art

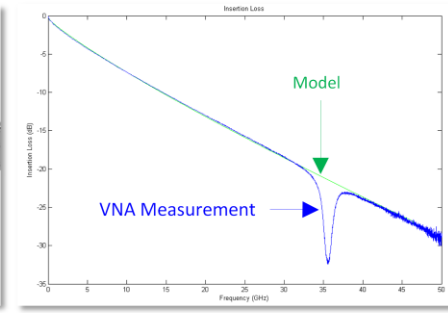


SEM Photo Reference [14]

Assumes stacked "snowballs" arranged in hexagonal lattice



11 spheres min; 38 spheres max of radius 1μm to fit within hex tile area and height of 5.8μm



Plot Reference [15]

Fit equation parameters to measured data

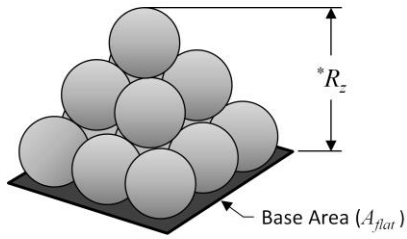
It is theoretically possible to build an accurate snowball model of the surface roughness by extracting parameters through detailed analysis of SEM photographs. But practically, it is beyond the capabilities of most companies who do not have access to such equipment. Even if such equipment was available, the size, number of spheres and general tooth shape must be approximated anyways.

Early versions of the snowball model attempted to replicate real world roughness profiles by building facsimiles of low and high profile tooth structures, using a stack of uniform spheres, as shown. Each sphere had a radius of less than 1μm to fit a stack height of less than 5.8 μm RMS because that was the dominant size of snowballs, as measured from SEM data.

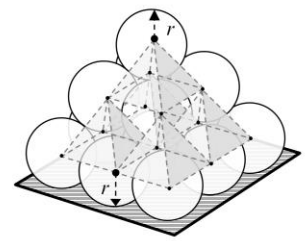
In this example, a hexagonal tile base, with a width of 9.4 μm RMS, was chosen to allow for replication into a lattice structure. Eleven spheres was the minimum number to fit within the hexagonal area and pyramid height of 5.8 μm RMS. Thirty-eight was the maximum number. By adjusting the number of spheres in this range shows excellent correlation to measurements.

Cannonball-Huray Model

Cannonball-Huray Model [3]



14 Spheres



$$r \approx \frac{R_z}{16.73}; A_{flat} = (6r)^2$$

$$K_{CH}(f) \approx 1 + 84\left(\frac{\left(\frac{\pi(r)^2}{A_{Flat}}\right)}{\left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2(r)^2}\right)}\right)$$

*R_z = 10-point mean roughness from data sheet

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This leads into what I like to call my Cannonball-Huray model. Using the concept of cubic close-packing of equal spheres, the spheres radius and tile area parameters for the original Huray model can now be easily estimated solely by the roughness parameters published in manufacturers' data sheets.

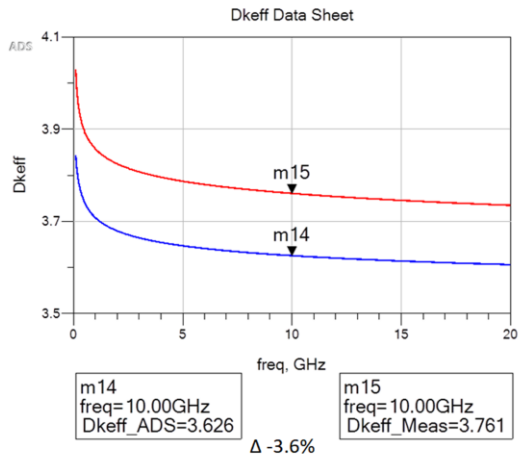
This model can be used to optimally represent the surface roughness. As illustrated on the left there are three rows of spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top. The height of the Cannonball stack is equal to the 10-point mean roughness R_Z as published in foil manufacturer's datasheets.

If we can peer into the stack, and visualize a pyramid lattice structure connecting to all the centers of the spheres, then the total height of the Cannonball stack is equal to the height of two pyramids plus two radii. Through simple geometry and a little bit of algebra we can approximate the radius of a single sphere $r = R_z/16.73$ and base area, $A_{flat} = (6r)^2$:

Because the model assumes the ratio of $A_{matte}/A_{flat} = 1$, and there are only 14 spheres, the Cannonball-Huray model can therefore be simplified by the equation as shown on the right: Where: $K_{SR}(f)$ = roughness correction factor, as a function of frequency; $\delta(f)$ = skin-depth, as a function of frequency in meters; r = the radius of spheres in meters; A_{flat} = base area in sq. meters.

Modeling D_{keff} Due to Surface Roughness

Dielectric Modeling Issue



When Data Sheet D_k is not the same as Effective D_k

Simulated with Keysight ADS [12]

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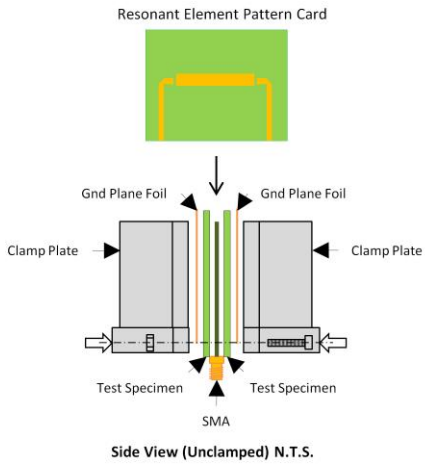
Everyone involved in the design and manufacture of printed circuit boards (PCBs) knows one of the most important properties of the dielectric material is D_k. When you compare simulation against measurements, you will often see a discrepancy in D_{keff}, due to increased phase delay caused by surface roughness.

In this case it is 3.6%

Clamped Stripline Resonator Test Method [13]



IPC-TM-650 test method used to rapidly test dielectric material for permittivity and loss tangent in a production environment

IPC-TM-650 - Section 2.5.5.5 - Rev C - Test Fixture [13]

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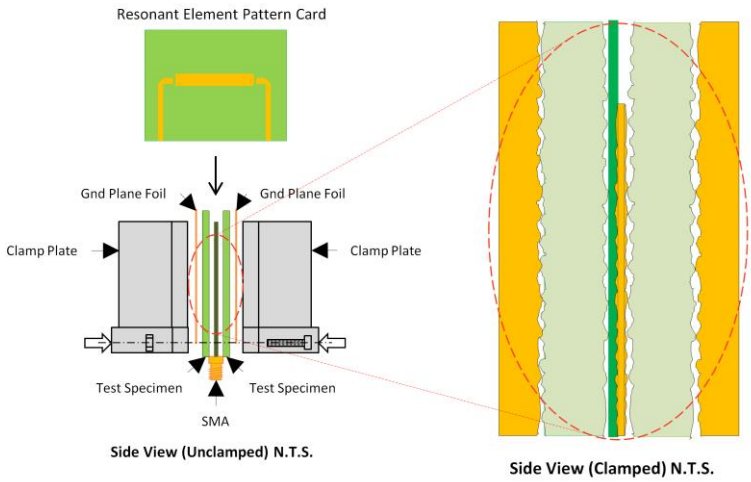
D_{keff} is highly dependent on the test apparatus and conditions of how it is measured. There are several methods used in the industry. One method, commonly used by many laminate suppliers, is a clamped stripline resonator test method, described by IPC-TM-650 Test Method.

IPC-TM-650, section 2.5.5.5, Rev C, defines test methods to rapidly test dielectric material for permittivity and loss tangent, over an X-band frequency range of 8-12.4 GHz, in a production environment. The measurements are made under stripline conditions using a carefully designed resonant element pattern card, made out of the same dielectric material to be tested. The card is sandwiched between two sheets of unclad dielectric material under test. The whole structure is then clamped between two large plates, lined with copper foils that are grounded. They act as reference planes for the stripline.

By measuring a resonant frequency of the cavity, the effective permittivity and loss tangent are determined. The value of this method is to assure consistency of product, when used in fabricated boards. It does not guarantee the values directly correspond to design applications.

Issues:



Since resonant element pattern card & material U.T. not physically bonded together => small air gaps between various layers & conductor roughness affects published results

Published D_k not same as D_{keff} due to roughness

IPC-TM-650 - Section 2.5.5.5 - Rev C - Test Fixture [13]

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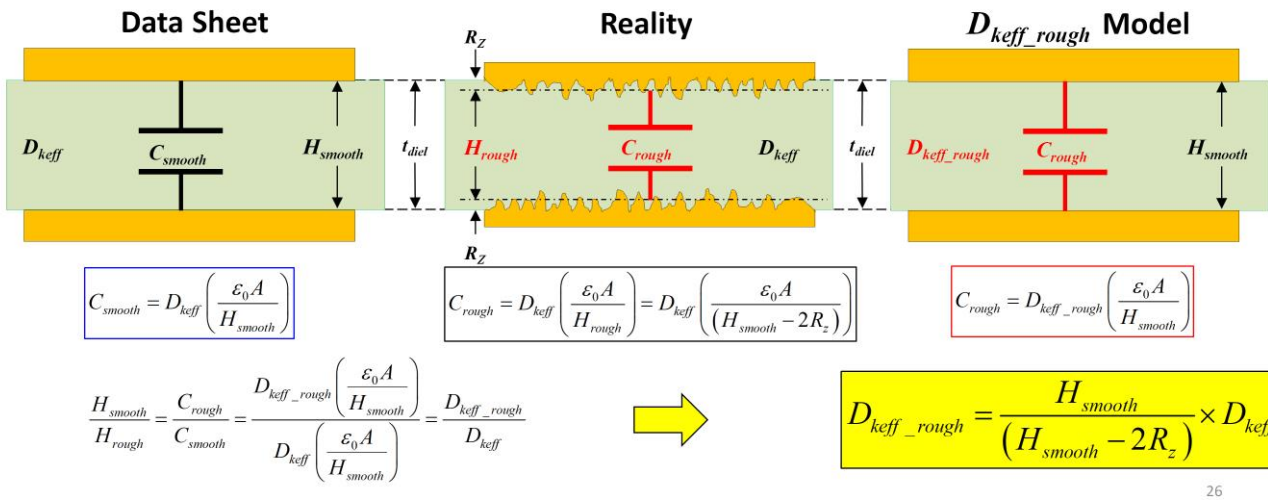
Therefore, Published D_k not same as D_{keff} due to roughness. This is a key point to keep in mind, and here is why.

Since the resonant element pattern card and material under test are not physically bonded together, as would be the case in real life, there are small air gaps between the various layers that affect measured results. These air gaps are caused, in part, by:

- Etching away the copper on material under test, leaving the bare substrate complete with the micro void imprint of the copper roughness
- The air gap between resonant element pattern card and material under test due to the copper thickness of the etch pattern
- The roughness profile of the copper, on the resonant element pattern card and fixture's grounded foil reference planes, are different than would likely be in practice.

D_{keff} Due to Roughness Model [1]

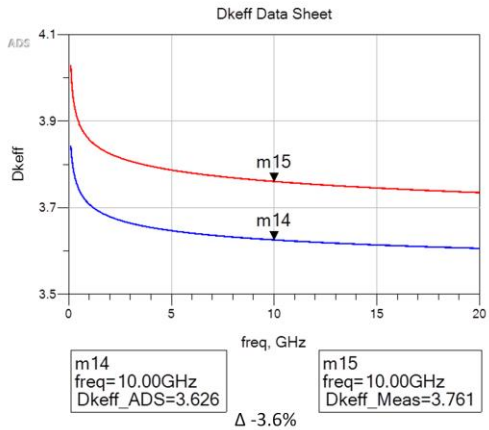


The illustration on the left shows an example of calculating capacitance between two smooth copper foil sheets bonded to each side of a dielectric material using dielectric thickness and D_{keff} from data sheets. The separation is denoted by H_{smooth} and is equal to thickness t_{diel}. If we know the cross-sectional area, D_{keff} and thickness, capacitance C_{smooth} is easily calculated.

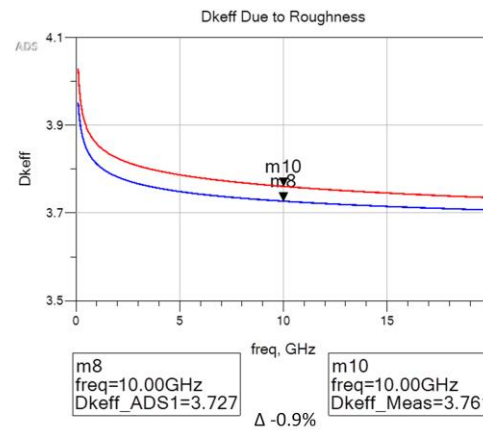
The reality is that when copper with roughness is actually bonded to the core, under heat and pressure, we see the rough copper tooth profile being pressed into the prepreg as shown in the middle illustration. The effective separation between copper sheets is less, compared to smooth copper model. If we assume the separation between the plates is reduced to (H_{smooth} -2Rz), then the capacitance due to roughness C_{rough} can be easily calculated by the middle equation shown.

Using D_{keff} with rough copper model in the middle, is equivalent to using D_{keff_rough} with smooth copper model, as shown on the right. If we do a little bit of algebra, we eventually come up with the simple equation, filled in yellow box, for D_{keff_rough}.This would then be used for impedance calculation and numerical simulations based on surface roughness, instead of effective D_k value published in manufacturers' data sheets.

FR408HR/RTF Simulation Results for D_{keff}



Data Sheet Values



D_{keff} Roughness Model

Simulated with Keysight ADS [12]

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For an FR408HR board with reverse treated foil, using data sheet values for *Dk*, we see that there is a difference of almost 4% between simulated and measured effective Dk at 10GHz . But when we correct the *Dk* due to roughness, we can improve the accuracy to within about 1%.

Model Validation

EDI CON 2017 Electronic Design Innovation Conference & Exhibition
Where high frequency meets high speed.

CMP-28 Test Platform

Photo courtesy Wild River Technology [6]

Features:

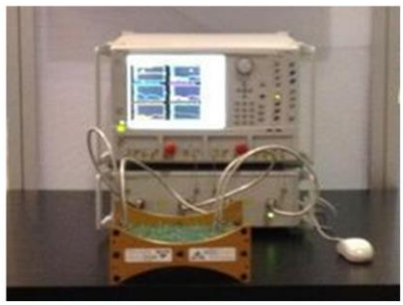
- FR408HR material with reverse-treated foil (RTF)
- Assembled with 2.92mm (CMP-28) or 2.4mm (CMP-32) connectors
- 3D EM benchmark structures
  - Loss structures for material extraction
  - Resonators for measurement correspondence
  - Multi-impedance structures for VNA time transform analysis

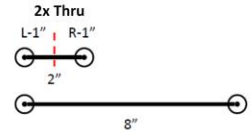
Applications:

- 3D-EM and measurement assistance for the SI practitioner
  - Vias
  - Multimode Analysis
  - Meshing Analysis Structure
  - Advanced Material Extraction and Loss Modeling
- THRU Calibration, T-matrix de- embedding
- Advanced Crosstalk analysis
- TRL/LRM Calibration Verification/Benchmark

The CMP-28 Channel Modeling Platform from Wild River Technologies was used for model validation. It is an excellent platform for model development and analysis. It contains a total of 27 microstrip and stripline interconnect structures. All are equipped with 2.92mm connectors to facilitate accurate measurements with a vector network analyzer (VNA).

Measure and De-embed for Generalized Modal S-parameters (GMS)





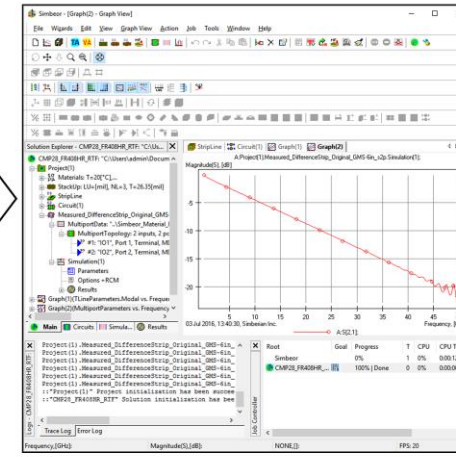
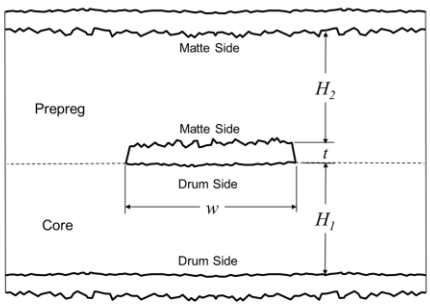


Photo courtesy Anritsu

Data courtesy Wild River Technology [6] & Simberian Inc. [7]

A VNA was used to measure a 2 inch, 2X thru, and an 8 inch long structure.
The 2X through structure was then de-embedded using Simbeor software.
A 6 inch GMS touchstone file was generated and used for later comparison.

FR408HR/RTF Data Sheet & Test Board Design Parameters [6],[8],[10]



Parameter	FR408HR/RTF
D_k Core/Prepreg @ f_o	3.65/3.59 @10GHz
D_f Core/Prepreg @ f_o	0.0094/0.0095 @ 10GHz
R_z Drum side	3.048 μm
R_z Before Micro-etch-Matte side	5.715 μm
R_z After 50 μin (1.27 µm) Micro-etch treatment -Matte side	4.445 μm
Trace Thickness, t	1.25 mils (31.73 μm)
Trace Etch Factor	60 deg taper
Trace Width, w	11 mils (279.20 μm)
Core thickness, H1	12 mils (304.60 μm)
Prepreg thickness, H2	10.6 mils (269.00 μm)
De-embedded trace length	6.00 in (15.24 cm)

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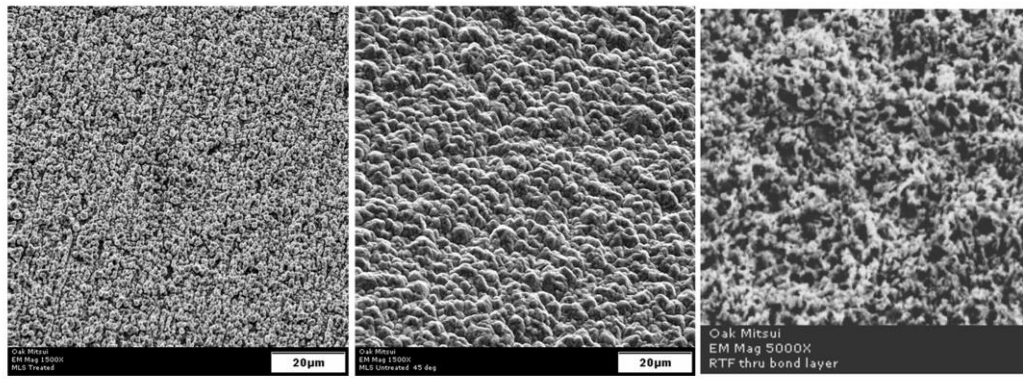
The data sheet and PCB design parameters are summarized in the Table. Respective *Dk*, *Df*, core, prepreg and trace thickness were obtained from data sheets.

MLS RT foil



Treated drum side	Untreated matte side	Matte side after etch treatment
Rz = 3.175 µm	**Rz = 5.715 µm**	**Rz = 4.443 µm**

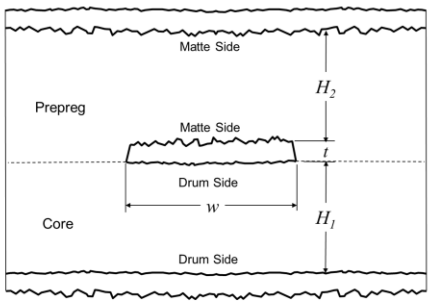
Photos courtesy of Oak-mitsui [10]

Here we see SEM photos of typical surfaces for MLS RT foil. The left and center photos are the treated drum side and untreated matte side respectively. The right photo is a 5000x SEM photo of the matte side after etch treatment showing micro-voids.

An oxide or micro-etch treatment is usually applied to the copper surfaces prior to final lamination. This provides enhanced adhesion to the prepreg material. Typically 50 µin (1.27µm) of copper is removed when the treatment is completed, depending on the board shop's process control. The etch treatment creates a surface full of micro-voids which follows the underlying rough profile and allows the resin to squish in and fill the voids providing a good anchor.

Because some of the copper is typically removed during the micro-etch treatment, the published roughness parameter of the matte side is reduced by nominal 50 µin (1.27 µm) for a new thickness of 175µin (4.445µm).

Determine D_{keff} Due to Roughness Core/Prepreg



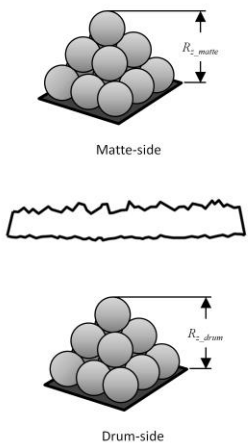
$$D_{keff_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_matte}\right)} \times D_{k_prepreg} = \frac{269\,\mu m}{\left(269\,\mu m - 2\times 4.445\,\mu m\right)} \times 3.59 = 3.713$$

$$D_{keff_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_drum}\right)} \times D_{k_core} = \frac{304.6\,\mu m}{\left(304.6\,\mu m - 2\times 3.048\,\mu m\right)} \times 3.65 = 3.725$$

33

The first step is to determine the effective *Dk* due to roughness for core and pre-preg.

Determine Sphere Radius (r) & Base Area (A_{flat})



$$r_{matte} \approx \frac{R_{z_matte}}{16.73} \approx \frac{4.443\mu m}{16.73} \approx 0.266\mu m$$

$$r_{drum} \approx \frac{R_{z_drum}}{16.73} \approx \frac{3.048\mu m}{16.73} \approx 0.182\mu m$$

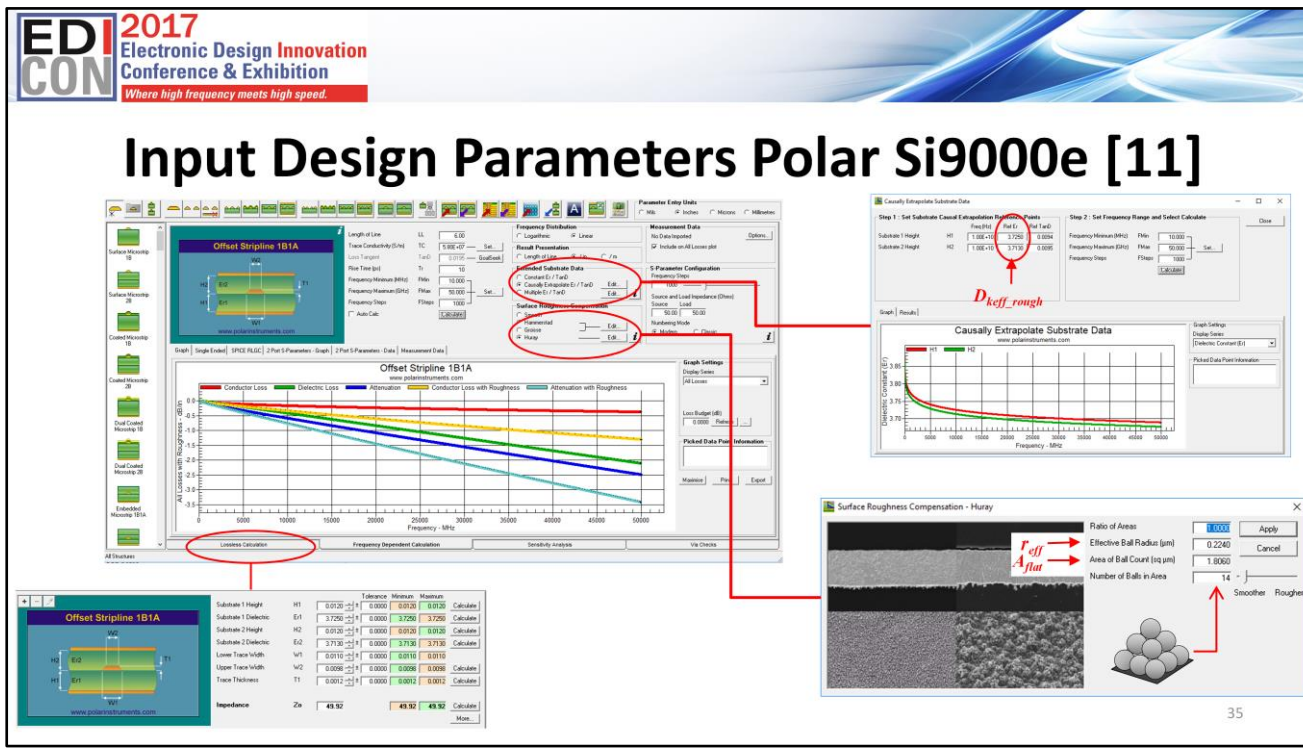
$$r_{eff} \approx \frac{r_{matte} + r_{drum}}{2} \approx \frac{0.266\mu m + 0.182\mu m}{2} \approx 0.224\mu m$$

$$A_{flat} = \left(6r_{eff}\right)^2 = (6 \times 0.224\mu m)^2 = 1.806\mu m^2$$

34

The next step is to determine the radius of spheres and base tile area for Huray model. Because electro-deposited (ED) foil has a matte side and drum side, with different roughness parameters, we must calculate the sphere radius for each side separately.

But most Huray models in EDA tools, including Polar Si900e, only allow one input for radius so I just take the average of the two for an effective radius (r_{eff}). Once we have that then it is easy to get the area (A_{flat}) of the flat tile base.



Here we see an example of Polar Si900e software main window and associated pop-up panels.

The first step is to select the “Lossless Calculation” tab at the bottom of the Si9000e main input window. When the pop-up window appears, choose the appropriate transmission line geometry from the pallet along the left-hand side, and then enter the specific design parameters in the boxes.

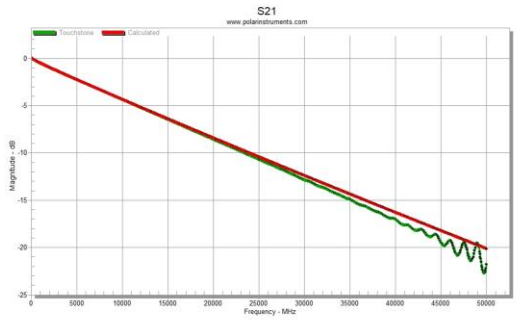
The next step is to select the “Frequency Dependent Calculation” tab at the bottom of the input panel and enter line length, conductivity and frequencies in the appropriate boxes in the main window.

Under the “Extended Substrate Data” section, choose “Causally Extrapolate Er / TanD” radio button and click “Edit” to enter the D_{keff} parameters in a pop-up window as shown. Click “Calculate” to view causal D_{keff} over frequency. Click “Close” to return to main window.

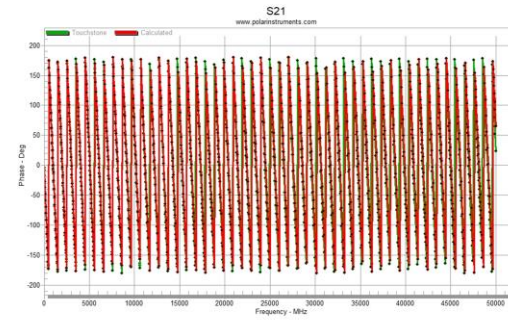
Under the “Surface Roughness Compensation” section from the main window, select Huray radio button and click “Edit” to enter the appropriate roughness parameters in the pop-up window. Enter r_{eff} and A_{flat} in the boxes shown. Enter 1.00 for “Ratio of Areas” and 14 for the “Number of Balls in Area” boxes. Click “Apply” to return to main window.

In the main window, hit calculate. Once the simulation has run, then export the touchstone file under the “File” menu if you want to save the s-parameters.

Simulated vs Measured



Insertion Loss



Phase

✓ Excellent Correlation!

Modeled and Simulated with Polar Si9000e [11]

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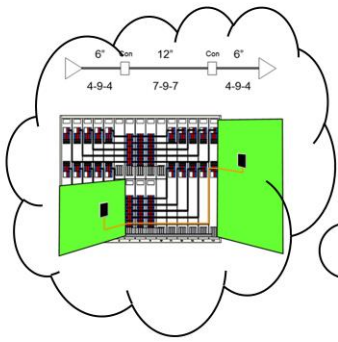
Here is the results of the simulation. As you can see there is excellent correlation for insertion loss and especially phase.



Well…single-ended looks great……BUT how well does this method work to model a practical backplane channel with diff pairs?

ExaMax Demonstrator Platform

- Design Intent - 28 GB/s NRZ
- Meg 6 or N4000-13EPSI Options
  - Nelco N4000-13EPSI Version Used
- MW-G-VSP ½ oz. foil (VLP)
- 2.9 mm coax connectors
- Case 1 = 8.25" (20.25") L12
- Case 2 = 14.80" (26.8") L10
- Case 3 = 20.22" (32.22") L10
- Case 4 = 26.70" (38.70") L12

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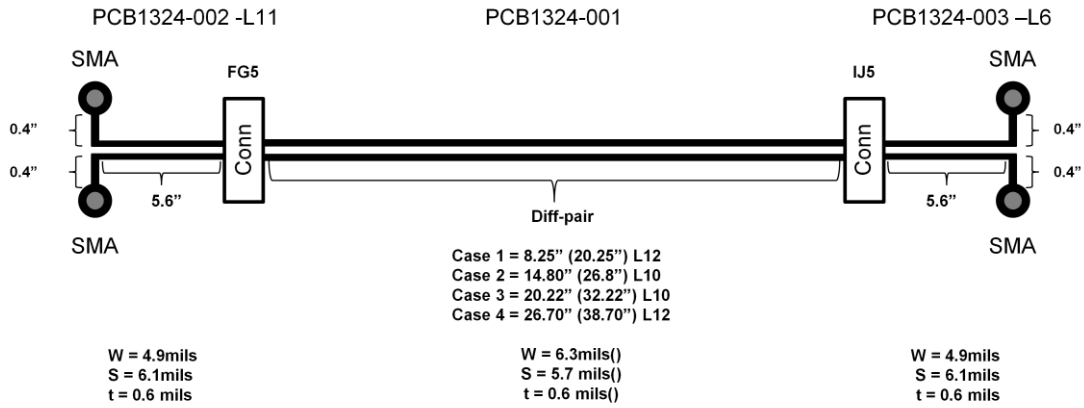
To demonstrate modeling High-speed channels, I will use the Amphenol-FCI Examax demo platform. This is a platform I helped design back in 2013 to showcase the Examax connector performance at 28GB/s NRZ. The Design Intent was to demonstrate 28 GB/s NRZ performance.

The same artwork supports Meg 6 or N4000-13EPSI material. Nelco N4000-13EPSI with MW-G-VSP ½ oz. foil (VLP) was used for this case study. The daughter cards used 2.9 mm coax connectors.

Four cases of different overall lengths were studied as shown.

Loss Topology Model N4000-13EPSI Summary



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This is a summary of the topology model. Both daughter cards were identical.

Breaking out of the coaxial connectors are 0.4 inches of single-ended trace before changing into 5.6 inches of differential pair routing. The backplane had 4 separate channels routed with various lengths shown.

Examax s-parameter models were also included.

Data Sheet Parameters [9], [10]

PARK ELECTROCHEMICAL CORP.

OAK-MITSUI Performance Copper Foils
MITSUI KINZOKU CORPORATE GROUP

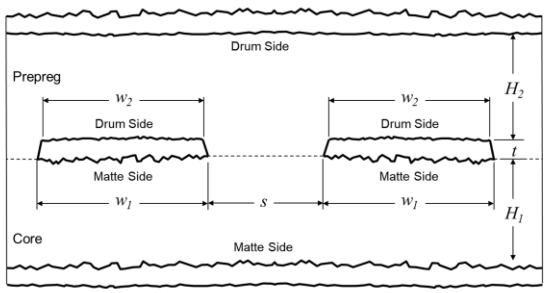
N4000-13 SI® / N4000-13EP SI® – Dielectric Properties Table

	Thickness & Tol.	Construction	RC%	2GHz Dk	2 GHz Df	10 GHz Dk	10 GHz Df
	0.0020 ± 0.0005	1 106	69%	3.04 ± 0.056	0.0082 ± 0.00021	3.02 ± 0.055	0.0086 ± 0.00023
	0.0020 ± 0.0005	1 1035	67%	3.07 ± 0.024	0.0081 ± 0.00009	3.04 ± 0.024	0.0085 ± 0.00010
	0.0025 ± 0.0005	1 1078	58%	3.19 ± 0.037	0.0077 ± 0.00014	3.16 ± 0.037	0.0080 ± 0.00016
	0.0030 ± 0.0005	1 1078	64%	3.11 ± 0.020	0.0079 ± 0.00007	3.08 ± 0.020	0.0083 ± 0.00008
	0.0025 ± 0.0005	1 1080	58%	3.19 ± 0.048	0.0077 ± 0.00018	3.16 ± 0.048	0.0080 ± 0.00020
	0.0030 ± 0.0005	1 1080	64%	3.11 ± 0.029	0.0079 ± 0.00011	3.08 ± 0.029	0.0083 ± 0.00012
	0.0035 ± 0.0005	1 2013	50%	3.29 ± 0.027	0.0072 ± 0.00010	3.27 ± 0.027	0.0075 ± 0.00011
DC Core	0.0040 ± 0.0005	2 1035	67%	3.07 ± 0.010	0.0081 ± 0.00004	3.04 ± 0.010	0.0085 ± 0.00004
	0.0040 ± 0.0005	1 2013	57%	3.19 ± 0.012	0.0076 ± 0.00005	3.17 ± 0.012	0.0079 ± 0.00005
	0.0040 ± 0.0005	1 2116	45%	3.38 ± 0.029	0.0069 ± 0.00011	3.35 ± 0.029	0.0072 ± 0.00012
	0.0050 ± 0.0007	1 2116	56%	3.21 ± 0.001	0.0076 ± 0.00000	3.18 ± 0.001	0.0079 ± 0.00001
	0.0050 ± 0.0007	2 1078	58%	3.19 ± 0.015	0.0077 ± 0.00006	3.16 ± 0.015	0.0080 ± 0.00006
	0.0060 ± 0.0007	2 1078	64%	3.11 ± 0.004	0.0079 ± 0.00002	3.08 ± 0.004	0.0083 ± 0.00002
	0.0050 ± 0.0007	2 1080	58%	3.19 ± 0.026	0.0077 ± 0.00010	3.16 ± 0.026	0.0080 ± 0.00011
BP Core	0.0060 ± 0.0007	2 1080	64%	3.11 ± 0.013	0.0079 ± 0.00005	3.08 ± 0.013	0.0083 ± 0.00006
	0.0070 ± 0.001	2 2013	50%	3.29 ± 0.027	0.0072 ± 0.00010	3.27 ± 0.027	0.0075 ± 0.00011

	Glass	RC%	2 GHz Dk	2GHz Df	10GHz Dk	10GHz Df	Thickness (inches)
	106	75	2.98	0.0084	2.95	0.0088	0.0025
	1035	75	2.98	0.0084	2.95	0.0088	0.0030
	1078	65	3.09	0.0080	3.06	0.0084	0.0032
BP/DC Prepreg	1080	65	3.09	0.0080	3.06	0.0084	0.0032
	2013	58	3.18	0.0077	3.15	0.0080	0.0044
	2116	55	3.22	0.0075	3.19	0.0078	0.0052

Here are the data sheet parameters highlighted with actual cores/prepregs used from the fabricator's stackup drawing.

ExaMax Demonstrator Platform
Data Sheet Design Parameters Summary



Parameter	N4000-13EPSI Backplane	N4000-13EPSI Daughter Card
D_k Core/Prepreg @ $10GHz$	3.08/3.06	3.04/3.06
D_f Core/Prepreg @ $10GHz$	0.0083/0.0084	0.0085/0.0084
R_z Matte side	2.5 μm	2.5μm
R_z Drum side	1.5 μm	1.5 μm
Trace Thickness, t	0.6 mils	0.6 mils
Trace Width, w_1	6.3 mils	4.9 mils (Diff) 5.4 mils (SE)
Trace Width, w_2	5.7 mils	4.3 mils (Diff) 4.8 mils (SE)
Trace Separation, s	5.7 mils	6.1 mils
Core thickness, H1	6 mils	4 mils
Prepreg thickness, H2	5.8 mils	5.8 mils

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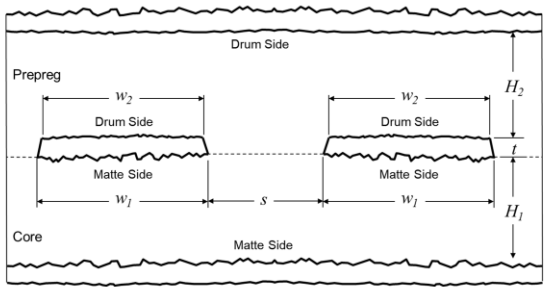
This is a summary of the transmission line geometry and design parameters from data sheets

Determine D_{keff} Due to Roughness Core/Prepreg



Daughter Card

$$D_{keff_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_drum}\right)} \times D_{k_prepreg} = \frac{6.2mils \times 25.4}{\left(6.2mils \times 25.4 - 2 \times 1.5\mu m\right)} \times 3.06 = 3.12$$

$$D_{keff_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_matte}\right)} \times D_{k_core} = \frac{4.0mils \times 25.4}{\left(4.0mils \times 25.4 - 2 \times 2.5\mu m\right)} \times 3.04 = 3.20$$

Backplane

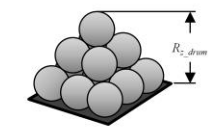
$$D_{keff_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_drum}\right)} \times D_{k_prepreg} = \frac{6.2mils \times 25.4}{\left(6.2mils \times 25.4 - 2 \times 1.5\mu m\right)} \times 3.06 = 3.12$$

$$D_{keff_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z_matte}\right)} \times D_{k_core} = \frac{6.0mils \times 25.4}{\left(6.0mils \times 25.4 - 2 \times 2.5\mu m\right)} \times 3.08 = 3.18$$

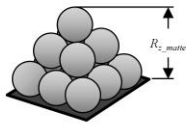
42

The first step is to determine the effective *Dk* due to roughness for core and pre-preg of daughter card and backplane.

Determine Sphere Radius (r) & Base Area (A_{flat})



Drum-side



Matte-side

$$r_{drum} \approx \frac{R_{z_drum}}{16.73} \approx \frac{1.5\mu m}{16.73} \approx 0.090\mu m$$

$$r_{matte} \approx \frac{R_{z_matte}}{16.73} \approx \frac{2.5\mu m}{16.73} \approx 0.149\mu m$$

$$r_{eff} \approx \frac{r_{matte} + r_{drum}}{2} \approx \frac{0.149\mu m + 0.090\mu m}{2} \approx 0.120\mu m$$

$$A_{flat} = (6r_{eff})^2 = (6 \times 0.120\mu m)^2 = 0.518\mu m^2$$

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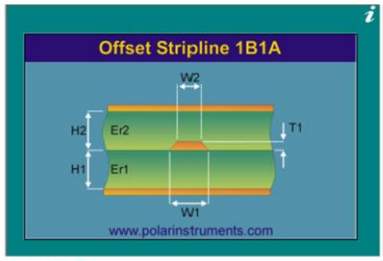
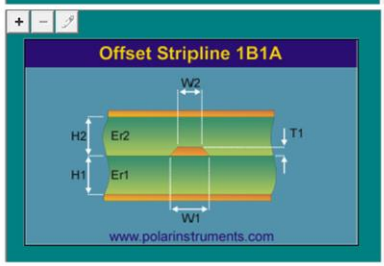
Similar to previous CMP28 Single-ended example, we determine the sphere radius and base area as shown.

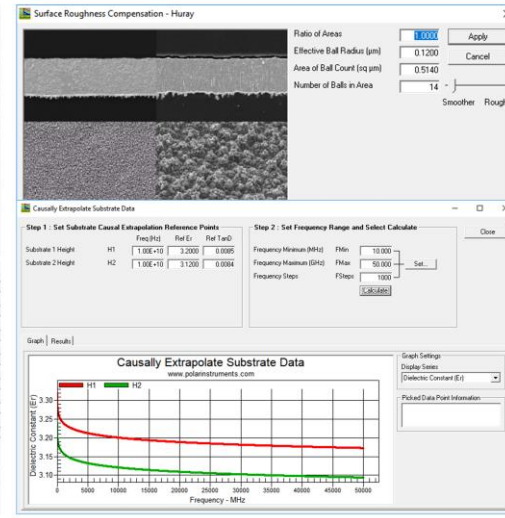
Polar ExaMax Daughter Card SE Trace Parameters



Length of Line	LL	400.00
Trace Conductivity (S/m)	TC	5.80E+07
Loss Tangent	TanD	0.0082
Rise Time (ps)	Tr	10
Frequency Minimum (MHz)	FMin	10.000
Frequency Maximum (GHz)	FMax	50.000
Frequency Steps	FSteps	1000
Auto Calc		Calculate



Substrate 1 Height	H1	4.0000
Substrate 1 Dielectric	Er1	3.2000
Substrate 2 Height	H2	6.4000
Substrate 2 Dielectric	Er2	3.1200
Lower Trace Width	W1	5.4000
Upper Trace Width	W2	4.8000
Trace Thickness	T1	0.6000
Impedance	Zo	49.06



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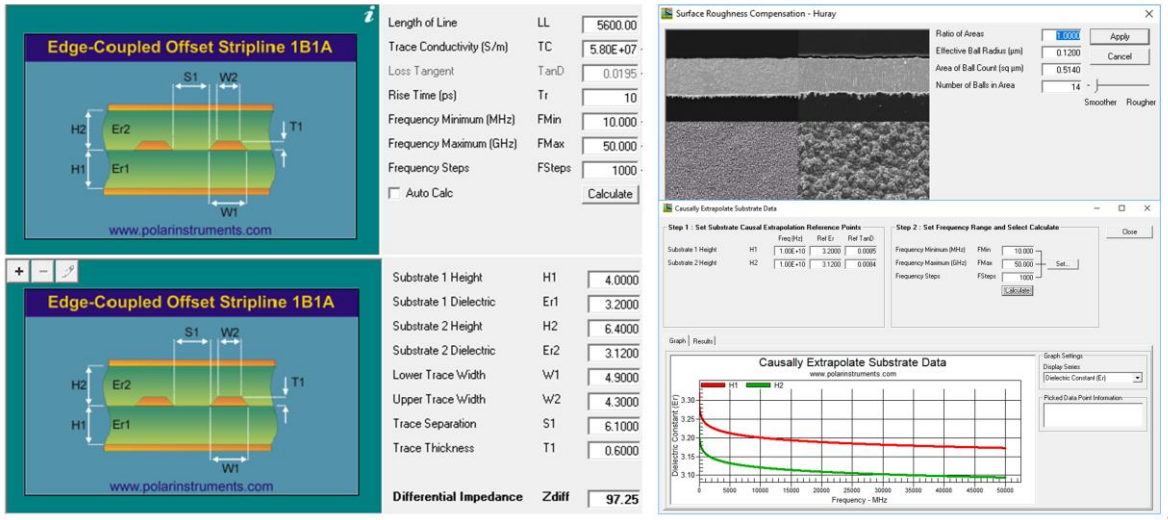
Here we enter the parameters for daughter card single-ended trace portion and save a touchstone file

Polar ExaMax Daughter Card Diff Trace Parameters



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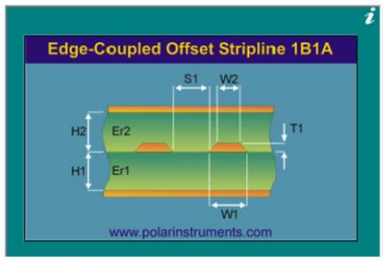
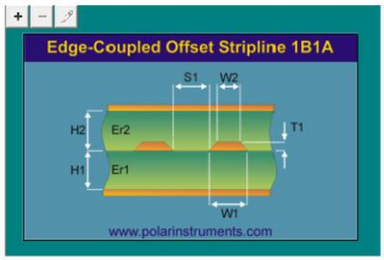
Then we enter the parameters for daughter card diff pair portion and save a touchstone file

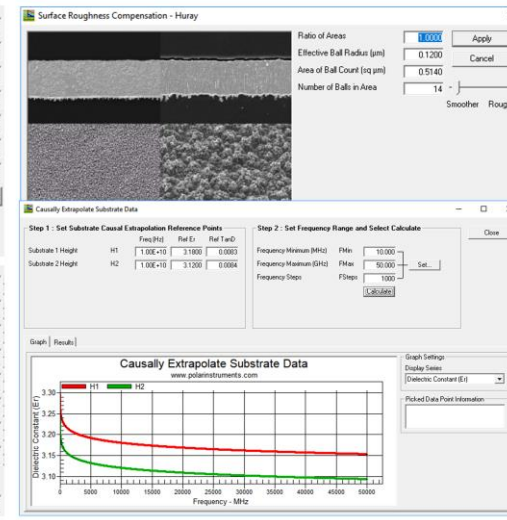
Polar ExaMax Backplane Diff Trace Parameters



Length of Line	LL **	8250.00
Trace Conductivity (S/m)	TC	5.80E+07
Loss Tangent	TanD	0.0195
Rise Time (ps)	Tr	10
Frequency Minimum (MHz)	FMin	10.000
Frequency Maximum (GHz)	FMax	50.000
Frequency Steps	FSteps	1000
Auto Calc		Calculate



Substrate 1 Height	H1	6.0000
Substrate 1 Dielectric	Er1	3.1800
Substrate 2 Height	H2	6.4000
Substrate 2 Dielectric	Er2	3.1200
Lower Trace Width	W1	6.3000
Upper Trace Width	W2	5.7000
Trace Separation	S1	5.7000
Trace Thickness	T1	0.6000
Differential Impedance	**Zdiff**	**93.88**

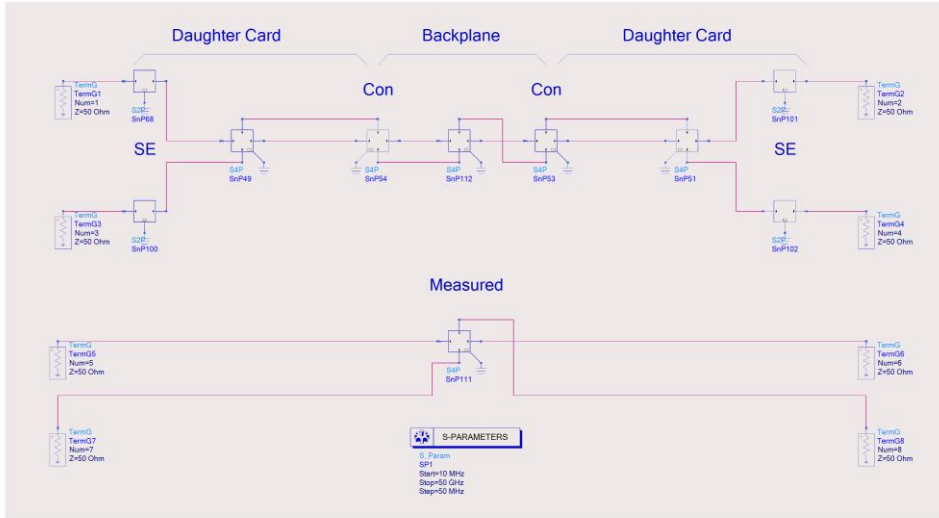


**Length of Line (LL) Adjusted for 8.25"; 14.80"; 20.22"; 26.70"

46

And finally we enter the parameters for backplane diff pairs. We do this for Case 1-4 and save a touchstone file for each

Keysight ADS [12] Generic Topology Model

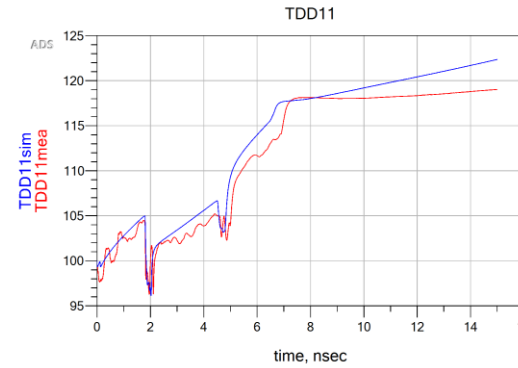


47

Keysight ADS is used to model and simulate the entire backplane channel, as shown here. The two schematics use the S-parameter pallet to model and compare the channel in the frequency domain.

All the Polar generated s-parameter files are concatenated together, as shown, including the Examax connector s-parameter files. Via and co-ax connector models are not included, because I want that "*OK answer NOW!*" You can always model and add them later to get that "*good answer late*." if need be.

ExaMax (R) Backplane Case 1 Total Length = 20.25”



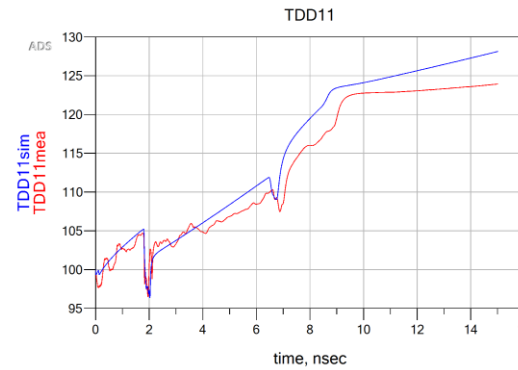
---- Measured
---- Simulated

48

And here are the results for Case 1. In the left is the differential insertion loss SDD21. On the right is the differential TDR plot TDD11.

Remarkably there is excellent correlation for insertion loss and impedance!

ExaMax Backplane Case 2 Total Length = 26.80”

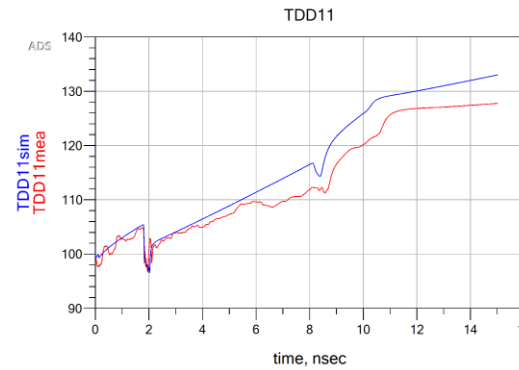


---- Measured
---- Simulated

49

Here are the results for Case 2. Similarly there is excellent correlation for insertion loss and impedance!

ExaMax Backplane Case 3 Total Length = 32.22”

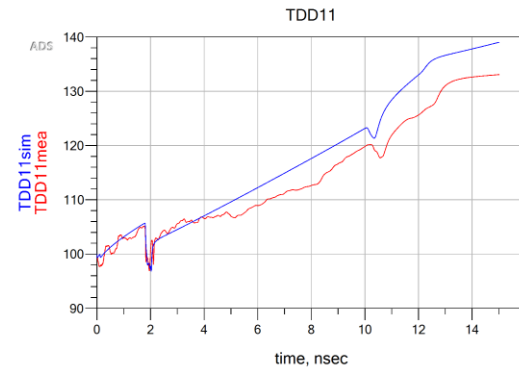


---- Measured
---- Simulated

50

Here are the results for Case 3. Still there is excellent correlation for insertion loss and impedance.

ExaMax Backplane Case 4 Total Length = 38.70”

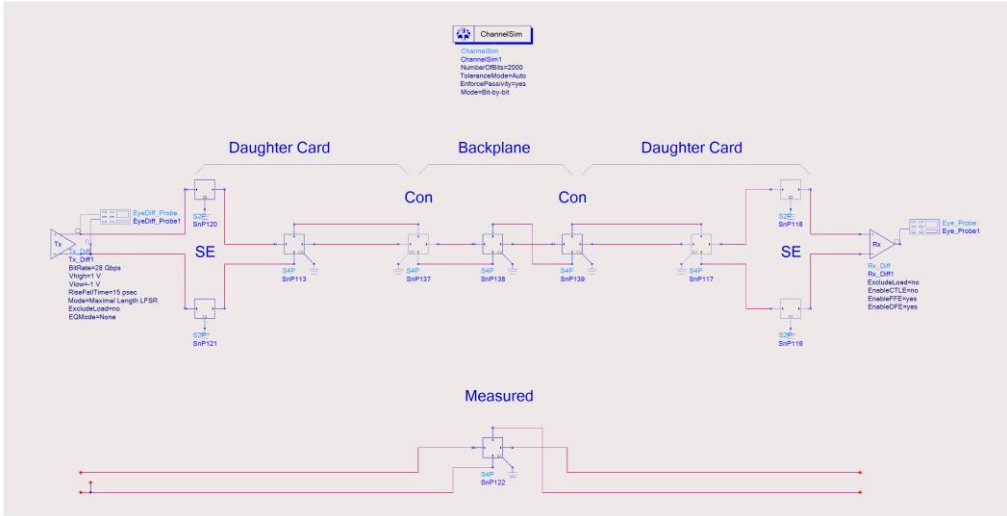


---- Measured
---- Simulated

51

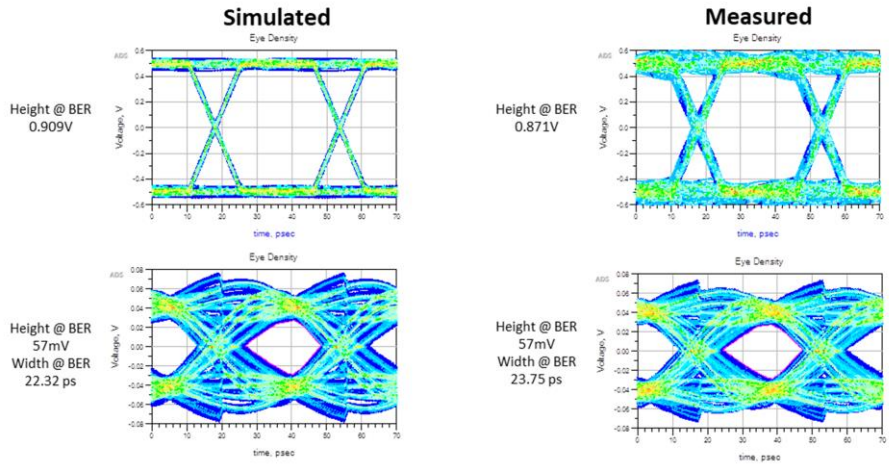
Finally here are the results for Case 4. Although there is slightly more loss than measured, there is excellent correlation for insertion loss and impedance.

Keysight ADS [12] Generic Channel Model



These two schematics use the “ChannelSim” pallet for transient simulation and eye diagram analysis.

Channel Simulation 28 GB/s Case 1 Total Length = 20.25”



Simulated with Keysight ADS [12]

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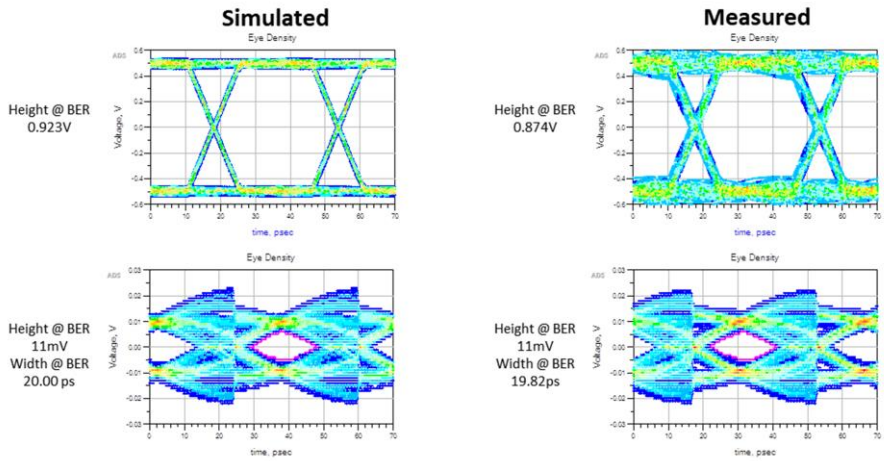
This slide shows plots of transmit eyes on top and receive eyes on bottom at 28GB/s. The simulated channel is on the left and the measured channel is on the right. Even though the measured transmit eye on the top right shows slightly more noise and jitter, the received eyes are virtually the same.

Channel Simulation 28 GB/s Case 4 Total Length = 38.7”



Simulated with Keysight ADS [12]

Similarly the longest length with slightly worse simulated loss shows virtually no difference in received eye opening suggesting the “*OK answer NOW!*” is probably good enough to make an engineering decision.

Summary

By using Cannonball-Huray model, with copper foil roughness and dielectric material properties obtained solely from manufacturers' data sheets, a practical method of modeling high-speed differential channels is now achievable using commercial field-solving software employing Huray model.

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Thank You!

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