Lamsim Enterprises inc.

Issue 02

# From Smooth to Imperfect Vias: The Rough Truth Impacting Simulation Model Accuracy

## White Paper

**Bert Simonovich**

**6/1/2025**

**Abstract:**

The anisotropy of glass-reinforced laminates influences dielectric properties along different axes, depending on the direction of the electric field. Beyond material anisotropy, factors such as resin content, fabricated dielectric thicknesses, and drilled hole size contribute to variations in the effective dielectric constant surrounding via structures. Additionally, via barrel roughness affects both Dkeff and time delay, further complicating accurate dielectric modeling. This study examines the challenges of determining true material anisotropy from via stub resonant structures and introduces a heuristic approach to improve via simulation model accuracy.

| DATE | ISSUE | DESCRIPTION |
|---|---|---|
| 5/25/2025 | 1.0 | INITIAL RELEASE |
| 6/01/2025 | 2.0 | CORRECTED FIG9 AND OTHER MINOR CORRECTIONS |
| | | |

Uncontrolled release. Latest issue can be found at Lamsimenterprises.com

# FROM SMOOTH TO IMPERFECT VIAS: THE ROUGH TRUTH IMPACTING SIMULATION MODEL ACCURACY

During DesignCon 2025 I had a number of side discussions with several people. We were discussing my DesignCon 2024 paper [1] on dielectric anisotropy, and how measured via test results they were measuring were not correlating well with the simulations when out-of-plane dielectric constant (Dkz) was converted to in-plane Dkxy using my heuristic method. From my paper, Isola's Tachyon 100G, material anisotropy averaged in the range of approximately 4-6% over different glass styles, while others claimed an anisotropy of 10-12% was required for accurate simulation correlation to measurement.

What's going on?

Well, there could be several reasons.

**The Short Answer:**

The anisotropy of glass reinforced laminates results in dielectric properties being different along the x, y, or z axis depending on the direction of electric field in the structure. Specifically, Dkxy refers to the case where the electric fields are parallel to the fiberglass cloth, while Dkz corresponds to the scenario where the electric fields are perpendicular to it. Determining material anisotropy is heavily dependent on the test fixture used to extract the properties.

In my paper [1], I defined percent anisotropy ($\Lambda$) as:

**Equation 1**

$$\Lambda \cong \left( \frac{Dkxy}{Dkz} - 1 \right) \times 100$$

Attempts have been made to extract dielectric anisotropy based on a quarter-wave resonant structure [5], [7] using a via acting as a stub. In principle this is a good idea. A quarter-wave resonant structure causes nulls in the S21 insertion loss (IL) plots as shown in Figure 1. The first resonant null at 13 GHz is the fundamental frequency ($f_0$) and nulls at every odd-harmonic thereafter. Given the speed of light ($c_0$), the length of the stub and the effective dielectric constant (Dkeff), surrounding the via hole structure, the resonant frequency can be predicted by:

**Equation 2**

$$f_0 = \frac{c_0}{4 \times stublength \times \sqrt{Dkeff}}$$

If we simply adjust Dk in our 3-D field solver to fit the measured results base on an as-fabricated printed circuit board (PCB) cross-section (x-section) dimensions and use it to calculate anisotropy from Equation

1, it is really only giving us an effective anisotropy (Λeff) to use in the model of a similar as fabricated via structure using the same dielectric material. It does not represent the bulk material anisotropy.

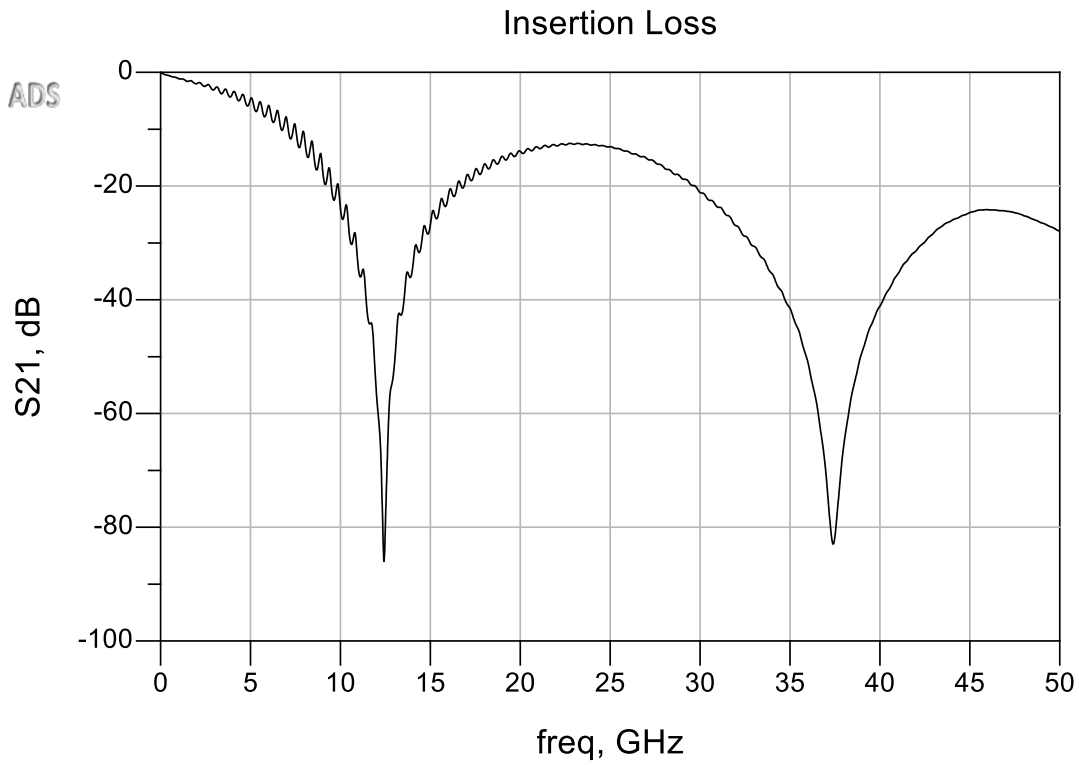


**Figure 1 S21 Insertion loss plot showing resonant nulls due to quarter-wave stub resonances.**

As I will show in this paper, material anisotropy is not solely responsible for contributing to Dkeff surrounding a via hole structure. You must also consider the as fabricated drilled hole size and resin content of the actual pressed thicknesses before applying my heuristic method to calculate Dkxy.

Finally, just as foil roughness affects Dkeff and phase or time delay (TD) in traditional PCB transmission lines, via barrel roughness influences the Dkeff surrounding it and increases TD. Since quarter-wave stub resonance is used to determine Λeff, an increase in Dkeff and TD lowers the resonant frequency, resulting in the perception of a higher anisotropy percentage.

**The Long Answer:**

Since Dkeff defined as the ratio of the actual dielectric structure's capacitance to the capacitance when the dielectric structure is replaced by air, Dkeff is directly proportional to capacitance. Furthermore, capacitance is also influenced by the electric potentials of surrounding metal structures. All 3-D field solvers account for this, so the only variation lies in what value of Dkeff is required for the model.

When modeling a via structure, we envision it as resembling the cross-section (x-section) illustration in Figure 2. In this example, the via barrels are perfectly smooth along their entire length. The antipads on each layer are aligned and symmetrical throughout the thickness of the PCB. The via barrel is surrounded by dielectric, and Dkeff is determined by the capacitance of the geometry. Many signal integrity (SI) engineers overlook the fact that all glass-reinforced laminates are anisotropic and instead they just use the

bulk Dk value provided in laminate suppliers' Dk/Df construction tables. They also assume that the final pressed thicknesses of the dielectric layers match the dimensions in the original as designed stackup drawing, and that the drill size specified in the computer-aided design (CAD) database corresponds to the actual size of the drill bit.

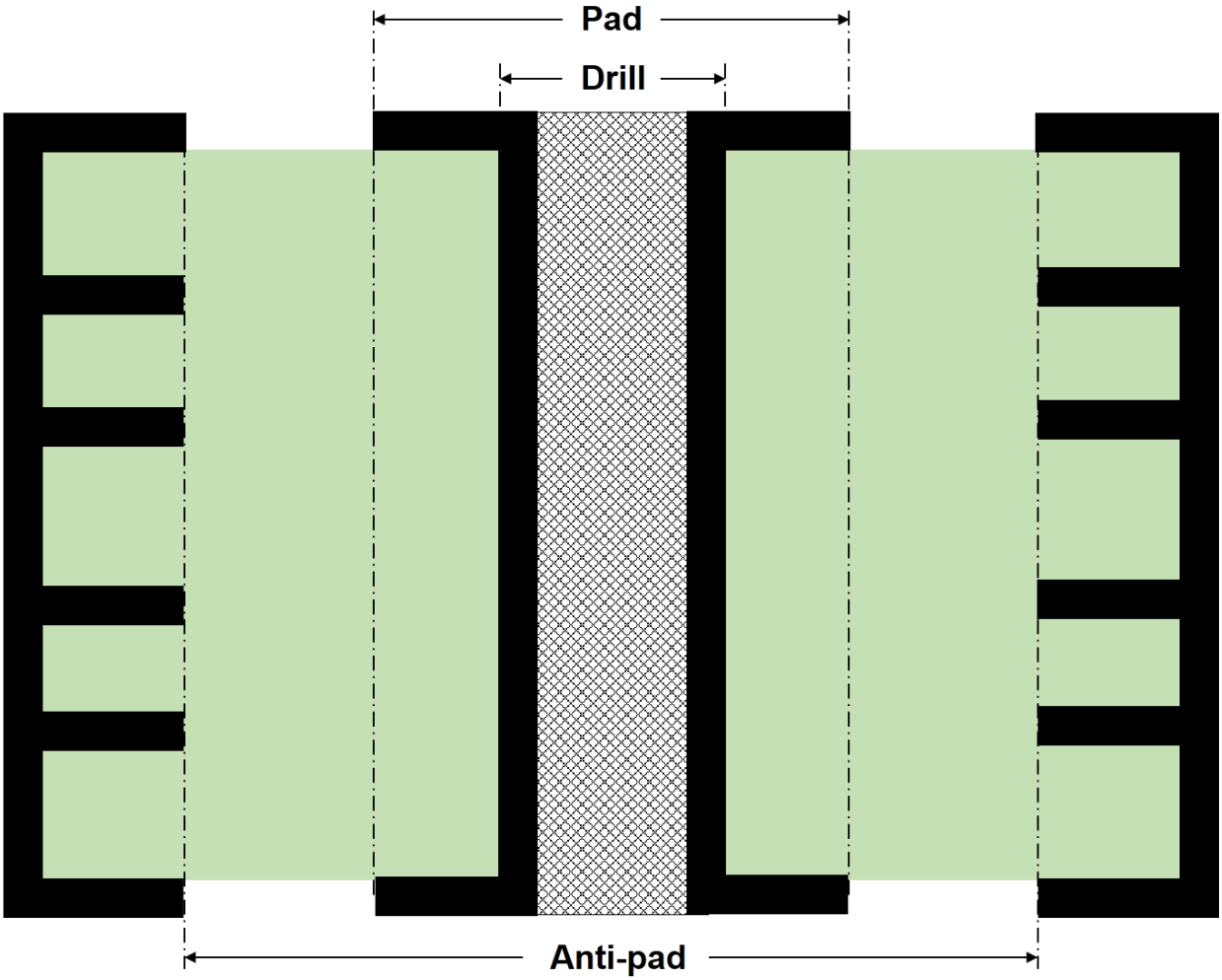


**Figure 2 Cross-section illustration example of an ideal via structure.**

But when we view an as fabricated x-section of a real via, we observe a different picture, as illustrated in Figure 3. In reality, the antipads are not always perfectly aligned layer to layer due to manufacturing tolerances. The via barrels are rough and often feature random whiskers protruding into the dielectric along its length. Since the via passes through a mixture of resin and fiberglass cloth, we need to use Dkxy value, which may differ from the bulk Dk published in the Dk/Df construction tables. The actual pressed thickness of the dielectric layers, measured from the x-section sample, can be different than the stackup drawing values used in the model. Furthermore, most CAD software specify the drill as finished hole size (FHS), not the actual drill diameter, which is the outer diameter of the via barrel. All these anomalies will affect Dkeff surrounding the via hole structure.

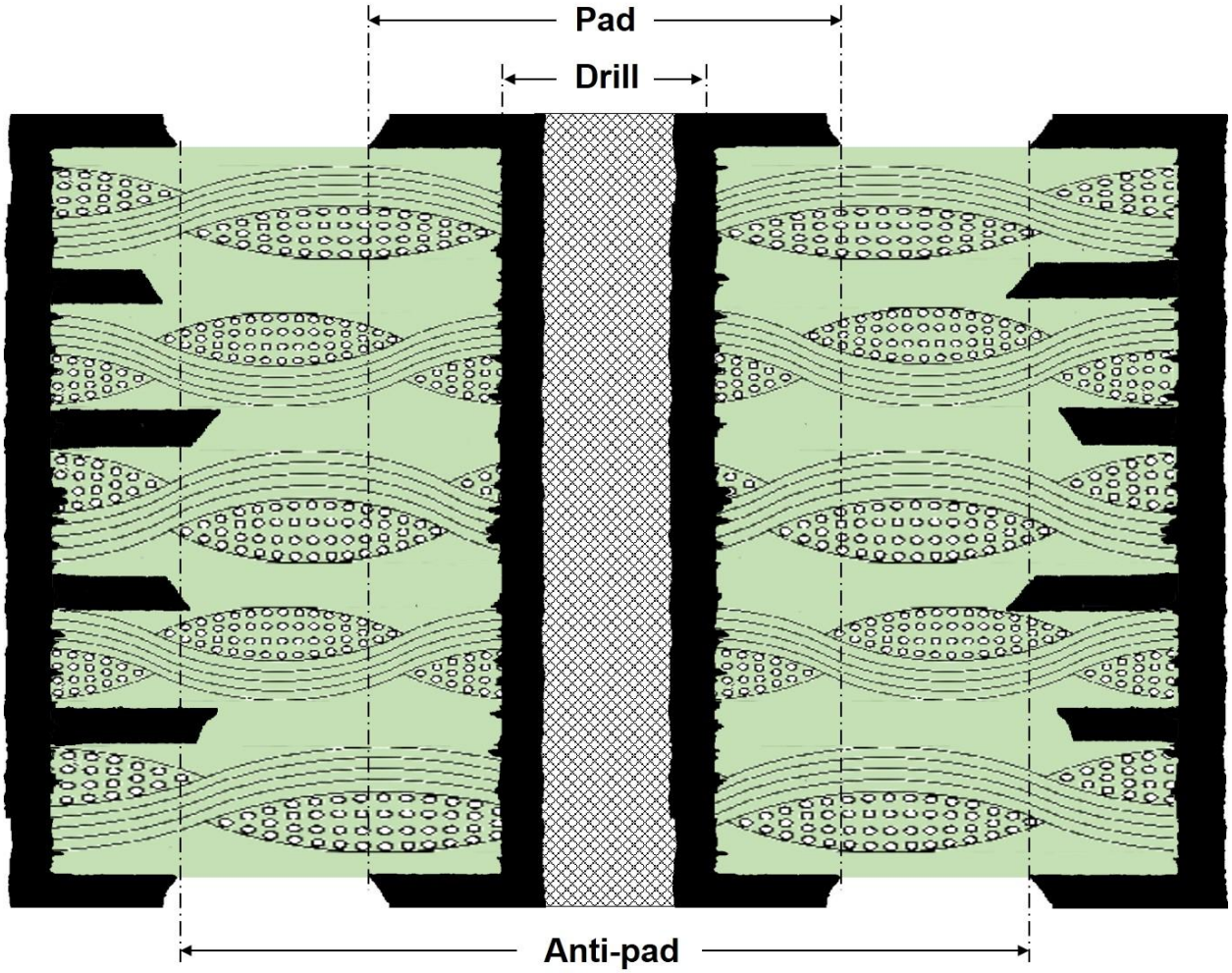


Figure 3 Cross-section illustration example of typical via structure as fabricated.

### Via Capacitance

In a true coaxial structure, as illustrated in Figure 4, the electromagnetic (EM) fields are completely contained within an outer ground (GND) shield that encloses a central conductor, separated by an insulating dielectric material. The electric field (E-field) determines capacitance and magnetic circular H-field determines the distributed via inductance. The mode of wave propagation is referred to as transverse electromagnetic mode (TEM).

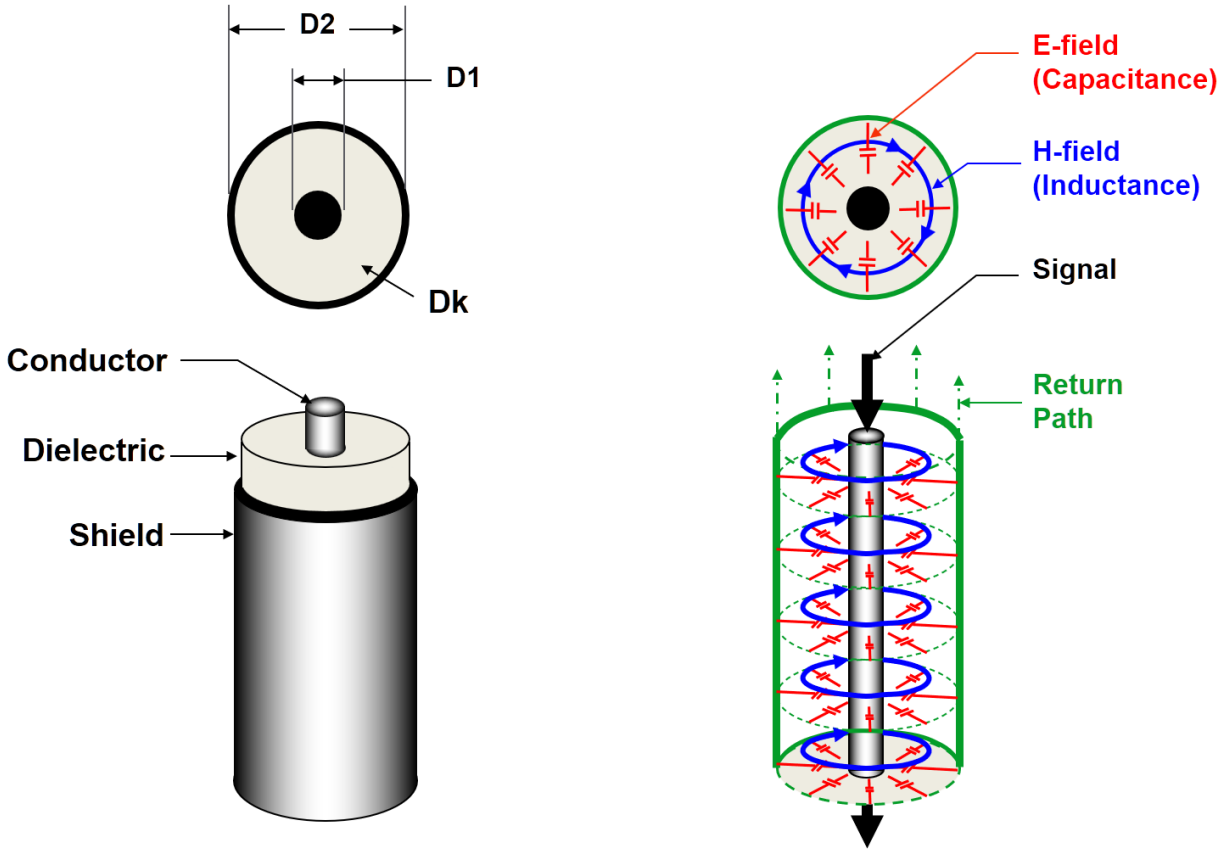


**Figure 4 Anatomy of a coaxial transmission line geometry and the electromagnetic field patterns with respect to TEM wave propagation through the structure.**

A closer look at the anatomy of the via structure is illustrated in Figure 3. Although it resembles a coaxial structure, the via is surrounded by anti-pad clearance holes in the ground (GND) reference planes, along with multiple GND vias, rather than a continuous shield. The GND vias localize the EM fields in the dielectric cavity between reference plane layers but they do not perfectly contain them, resulting in quasi-TEM wave propagation.

In Figure 5 Section A-A, the electric field determines capacitance and are represented as distributed via capacitance (Cvia). Magnetic circular H-field determines the distributed via inductance (Lvia). For a multi-layer PCB structure with several GND reference planes distributed evenly throughout the thickness, as illustrated in Figure 5 example, the via capacitance is mainly influenced by the drill size (Drill$\phi$), antipad diameter (Antipad$\phi$) and to some extent any GND vias in close proximity.

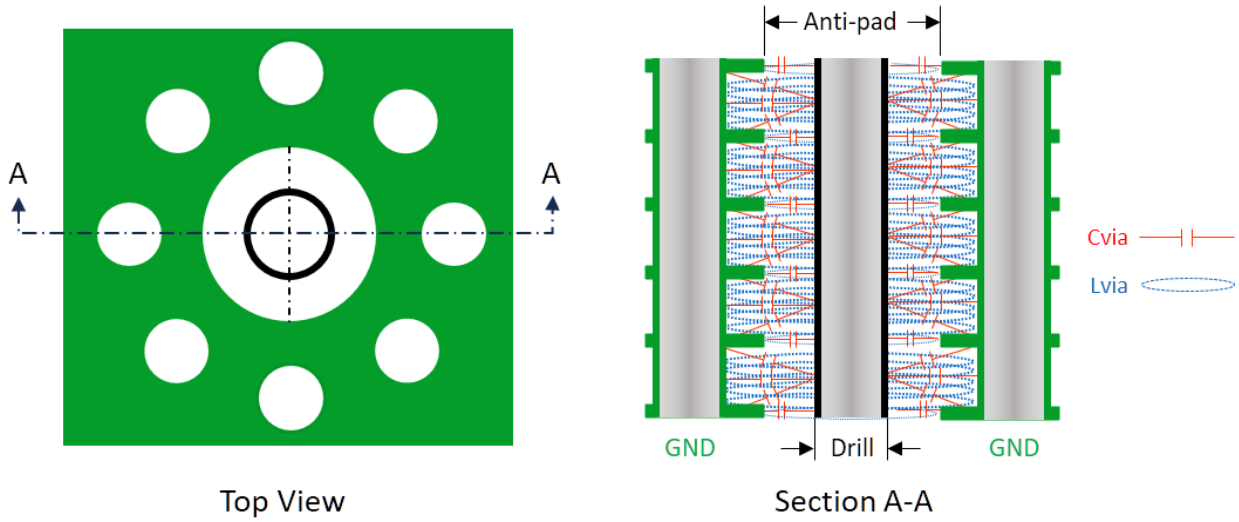


**Figure 5 Anatomy of a single via structure surrounded by GND reference vias**

Thus, the via capacitance can be approximated using Equation 3. We see that increasing the drill diameter or decreasing the antipad diameter results in a higher capacitance, since the space between the outer diameter of the via barrel and the diameter of the antipad becomes smaller.

**Equation 3**

$$Cvia \cong \frac{2\pi\varepsilon_0}{\ln\left(\frac{Antipad\phi}{Drill\phi}\right)} \times Dkxy$$

where:

Cvia = capacitance of via in F/per unit length

$\varepsilon_0$ = permittivity of free space = 8.854 pF/m or 0.225 pF/inch

Dkxy = in-plane dielectric constant

Antipadϕ = antipad diameter

Drillϕ = drill diameter

CAD software defines FHS in the PCB layout. To add to the confusion, some CAD software also call this drill size. Fabrication notes will specify actual drill diameter tolerances and the board shop will adjust these to meet plating hole thickness depending on PCB class the design has to meet. The actual drill diameter is at least 2 mils larger than the FHS but may be 3-4 mils larger depending on the plating requirements specified. When engineering design automation (EDA) tools import the design database for SI analysis, it is the FHS that gets imported. This is a common trap SI engineers fall into when modeling vias, and using the FHS instead of actual drill size will under estimate via capacitance and thus Dkeff.

Non-functional (NF) pads (not shown) are pads attached to the via on layers that serve no function. In other words, they do not connect to any traces. Years ago, they were included because it was thought they improved via mechanical reliability and had little effect on the signal integrity of the time. Including non-functional pads will decrease the space between the pad's outer diameter and the diameter of the antipad, thus increasing capacitance, unless the antipads are enlarged to compensate. Today, milti-gigabit designs specify non-functional pads to be removed to mitigate excess capacitance. Ideally this is done in the original artwork, but sometimes it is left to the PCB fabricator to remove them before fabricating. If the fabrication notes are poorly communicated, then you could end up with NF pads resulting in poor SI correlation to measurements. Unless you do a micro-section, you will not know and draw the wrong conclusions.

**Via Roughness**

Roughness of the via barrel is mainly caused by copper platting wicking into voids in the drilled hole caused by drill bit crazing the glass reinforcement weave, and is usually caused by a dull drill bit. It is usually not considered when modeling a via, but is a factor when trying to do SI correlation.

Figure 6 is an illustration showing a blowup of copper plating wicking into the glass bundles. IPC-600G [4] defines acceptable amount of wicking allowed depending on the class the PCB has to meet. It can be as high as 125 µm (4.291 mils) for Class 1 to as low as 80 µm (3.15 mils) for Class 3.

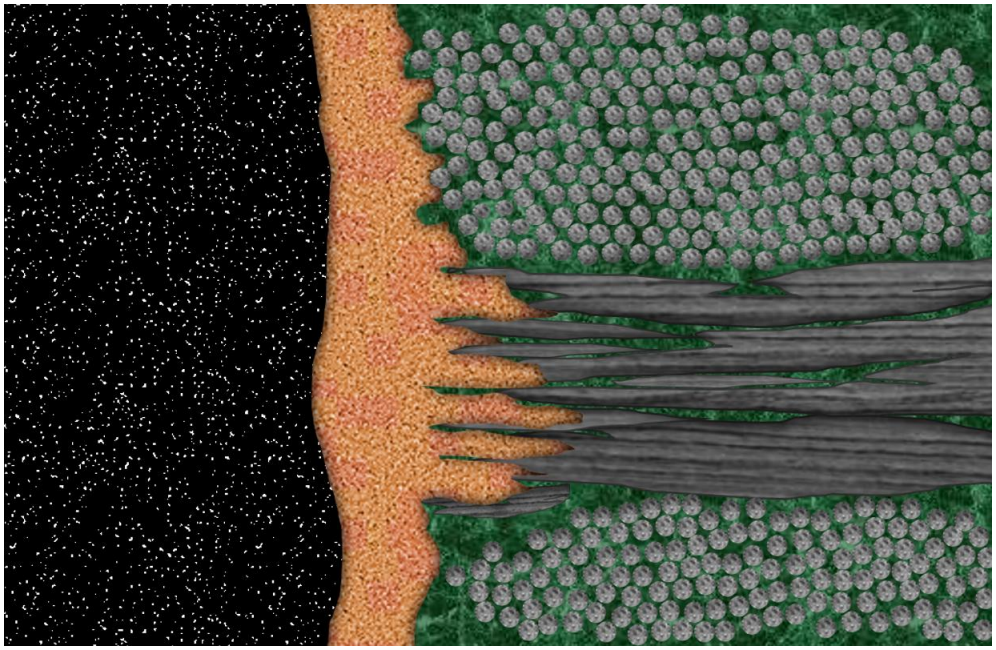

**Figure 6 Copper plating wicking into glass crazing caused by drill bit.**

Via barrel conductor roughness has the same effect on increasing via capacitance resulting in higher Dkeff in the same way copper surface roughness increases self-capacitance (C11) of transmission line geometries [2]. Since wicking extends past the actual drill diameter it concentrates the electric fields and increases capacitance.

This is validated by HFSS simulations, as shown in Figure 7. Figures (A) and (B) show color maps of E-field strength in cross-section for perfectly smooth and rough vias, respectively. As seen in the images, the E-field is primarily contained within the anti-pad opening of the reference planes, similar to its behavior in a perfect coaxial geometry. In this example, we observe increased E-field strength along the roughness profile in Figure (B), leading to a 2.6% increase in capacitance.

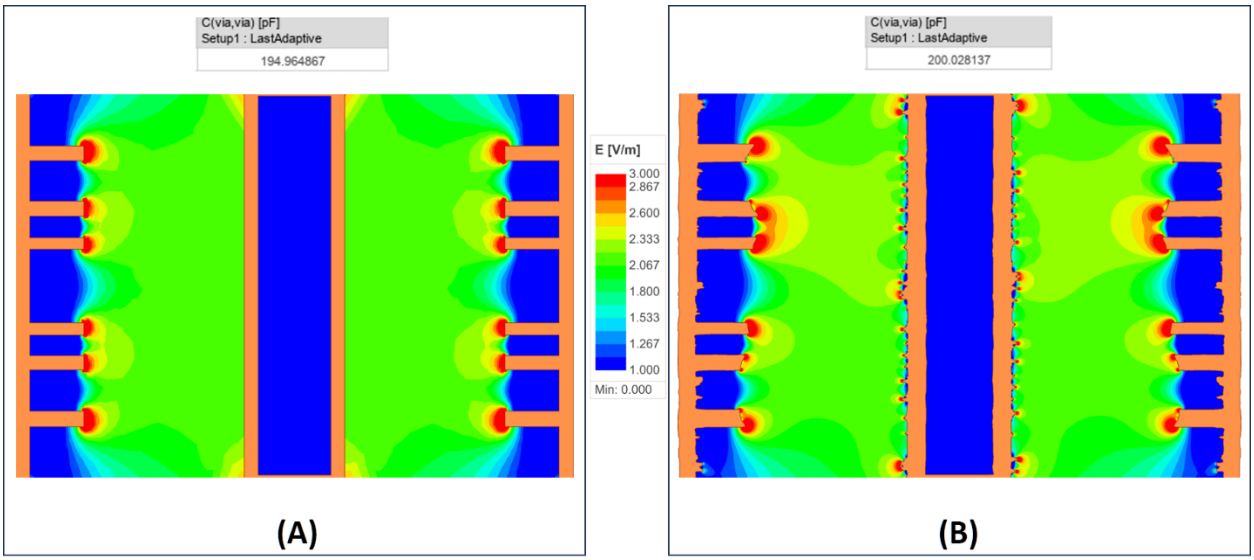


**Figure 7 Electric field strength color map and capacitance of smooth vias (A) and rough vias (B). Simulations courtesy of Juliano Mologni, Ansys.**

Unfortunately, achieving model correlation with via measurements is challenging due to the randomness of wicking and the via's passage through the mixture of glass and resin. A single cross-section is insufficient because it represents only one slice of a 360-degree hole where wicking can be random anywhere around the circumference. For example, Figure 8 is a microscopic top-down view of a slice of an actual plated through hole showing copper wicking into the glass weave faintly visible running horizontal and vertical in the picture. By inspection we imagine slicing the via horizontally exactly at the maximum diameter would not have captured the maxim amount of wicking. It's is also hard to measure exact via diameter after cross-sectioning because there is no guarantee the microsection was accurately cut at the maximum diameter. Depending on how square and accurate the cutting and polishing was, there can be slight variations in diameter.

**Dkeff Compensation Due to Conductor Roughness**

As shown in Figure 8, the measured inner ring diameter of 14.4 mils (365.8 µm) represents the FHS. The middle ring drill diameter is 18.43 mils (468.1 µm). By inspection, the outer ring diameter of 18.80 mils (477.50 µm) represents the drill diameter plus the average roughness. It should be noted that, because a via is round, it is analogous to a flat sheet of foil wrapped into a circle. Therefore, the actual surface conductor roughness is half the difference between the drill diameter and the average roughness diameter. In this case, the average surface roughness is calculated as 0.5 × (18.80 - 18.43), which is approximately 0.2 mils (5 µm)..

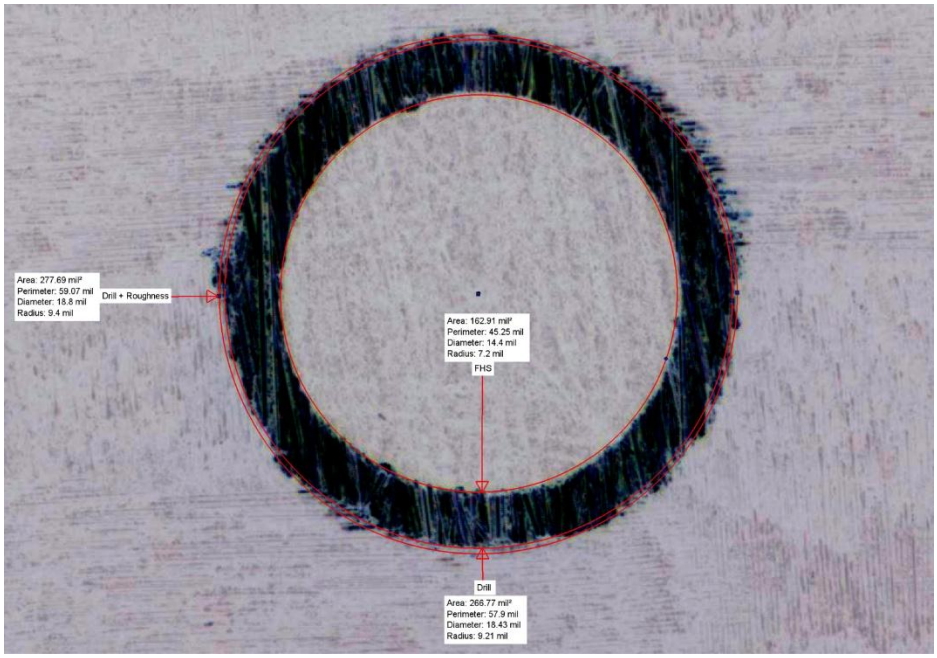


**Figure 8 Microscopic top-down view of a slice of an actual plated through hole showing copper wicking into the glass weave faintly visible running horizontally and vertically.**

Heuristically, we can estimate additional capacitance and Dkeff correction due to roughness for via example in Figure 8. If the ratio of $Dkeff_{rough}$ to $Dkeff_{smooth}$ is defined as:

**Equation 4**

$$\frac{Dkeff_{rough}}{Dkeff_{smooth}} = \frac{Cvia_{rough}}{Cvia_{smooth}}$$

From Figure 8, if Drill$\phi$smooth = 18.43 mils; Drill$\phi$rough = 18.80 mils and assuming a typical antipad diameter of 40 mils, then by combining Equation 3, with Equation 4, $Dkeff_{rough}$ can be expressed by Equation 5. When plugging in the numbers, we see $Dkeff_{smooth}$ increases by 2.6% as compared to Dkeffsmooth.

**Equation 5**

$$Dkeff_{rough} = \frac{Cvia_{rough}}{Cvia_{smooth}} \times Dkeff_{smooth} \cong \frac{\ln\left(\frac{Antipad\phi}{Drill\phi_{smooth}}\right)}{\ln\left(\frac{Antipad\phi}{Drill\phi_{rough}}\right)} \times Dkeff_{smooth}$$

$$\cong \frac{\ln\left(\frac{40}{18.43}\right)}{\ln\left(\frac{40}{18.80}\right)} \times Dkeff_{smooth}$$

$$\cong 1.026 \times Dkeff_{smooth}$$

Via stub test vehicles are commonly used for SI model validation [5], [7]. Via stubs are quarter-wave resonant structures that depend on TD, determined by the stub length, which is equivalent to one quarter of the period (T) of the resonant frequency. The common practice to extract Dkeff from the first quarter-wave resonant frequency null from an S21 IL plot similar to Figure 1 is:

**Equation 6**

$$Dkeff = \left( \frac{c_0}{4 \times stublength \times f_0} \right)^2$$

But Equation 6 assumes that Dkeff is entirely determined by capacitance. However, for time-variant electromagnetic fields, inductance also contributes to time delay (TD). Via barrel roughness affects the self-inductance (L11) in the same way that copper surface roughness increases L11 in transmission line geometries. In my previous paper [3], Dkeff for time-variant electromagnetic fields is expressed as:

**Equation 7**

$$Dkeff = c_0^{\,2} \left( L_{11} C_{11} \right)$$

where: $c_0$ = speed of light; L11 = Self-inductance; C11 = Self-capacitance.

Equation 7 clearly demonstrates that an increase in L11 leads to a proportional increase in Dkeff. Failure to use software that incorporates a causal metal roughness model, such as the Bracken model [8], to account for inductance caused by conductor roughness can result in misinterpreting the extracted Dkeff value and misunderstanding the impact of anisotropy.

To validate my hypothesis, I reached out to my friend, Juliano Mologni from Ansys for some help with an experiment to add roughness to a via ¼ wave stub structure. The goal was to see if we can observe any measurable change in resonant stub frequency and thereby quantify its effect on extracted Dkeff using Equation 6.

He created a simple six layer via stub structure in HFSS, as shown in Figure 9. The drill diameter was 10 mils (254 um), antipad diameter was 50 mils (1.27 mm) and six stitching vias equally spaced at 60 mils (1.52 mm) diameter as shown. The port 1 – port 2 feed traces were on the top layer to achieve a maximum via stub length of 150 mils (3.81 mm). Dielectric Dk was 3.97.

We used the Huray roughness model, incorporating the causal Bracken model, to account for added inductance due to conductor roughness. The Huray nodule radius (NR) was parameterized from 0 to 2 µm (78.7 µin) in 0.1 µm (3.94 µin) increments. Based on my Simonovich Cannonball roughness model [9], which stacks 14 spheres, the Hall-Huray surface ratio (SR) parameter remains constant at 4.9. Converting NR to Rz roughness is straightforward and simply calculated as:

**Equation 8**

$$Rz \cong \frac{NR}{0.06}$$

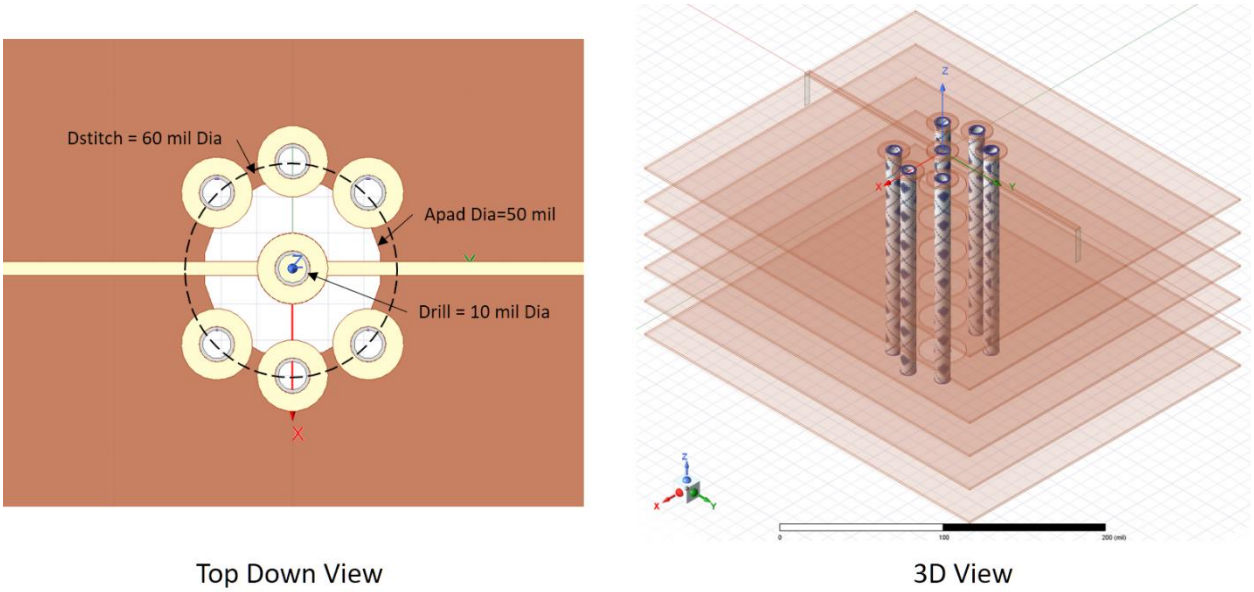


**Figure 9 HFSS via stub model showing roughness added to all vias. HFSS simulation model courtesy of Juliano Mologni, Ansys.**

Figure 10 plots the S21 IL showing the quarter-wave stub resonant nulls for 0-2 µm Huray NR roughness parameters. The resonant frequency was measured for each NR parameter and converted to Dkeff using Equation 6. Equivalent Rz was also calculated using Equation 8. This would translate to 0-33 µm Rz equivalent roughness.

Since the Bracken model only corrects the imaginary part of the complex impedance of the rough metal, it does not correct the capacitance, so the increased Dkeff change is solely due to increased L11.

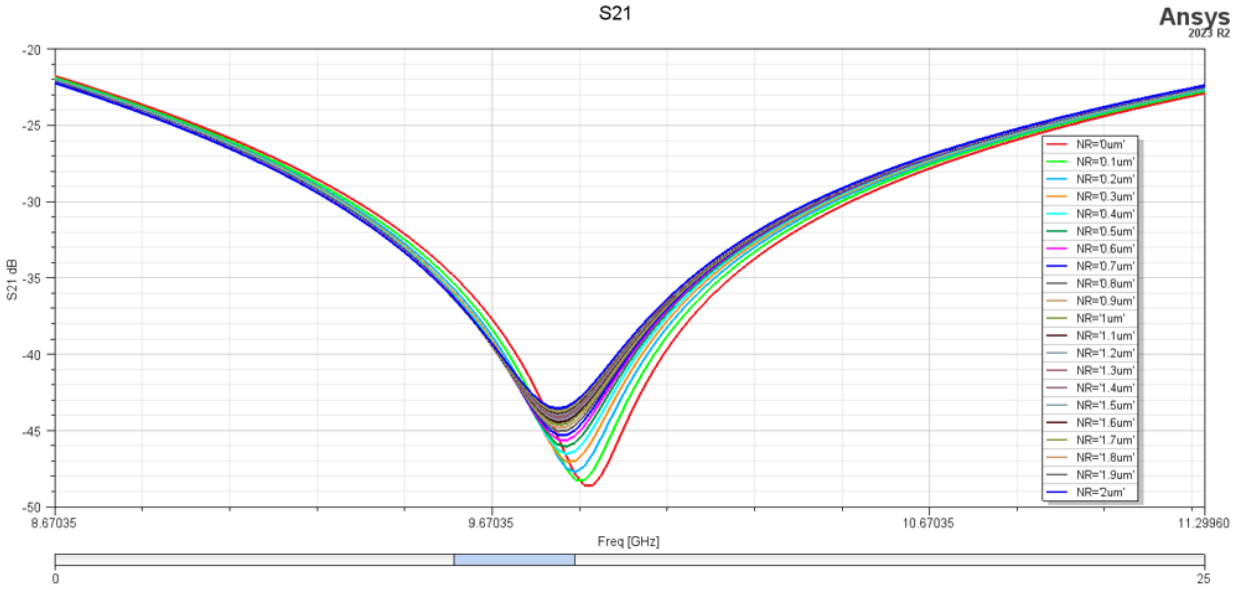


**Figure 10 S21 IL showing the quarter-wave stub resonant nulls for 0-2 µm Huray nodule radius (NR) roughness parameters. Simulation courtesy of Juliano Mologni, Ansys.**

Figure 11 summarizes the simulated results in the table and the graph plots Dkeff vs Rz roughness columns. By observing the third-order polynomial fit, we observe an exponential change in Dkeff and levels off at 4.03. This was surprising observation and further investigation to explain why it levels off was not done. None the less, the simulation results confirm our hypothesis and a Rz roughness of 10 µm seems reasonable average via barrel surface roughness.

| $f_0$ | TD ps | NR um | Rz um | Dkeff | Dkeff % Delta |
|---|---|---|---|---|---|
| 9.900E+09 | 25.253 | 0.0 | 0.000 | 3.96744 | 0.00% |
| 9.880E+09 | 25.304 | 0.1 | 1.667 | 3.98352 | 0.41% |
| 9.860E+09 | 25.355 | 0.2 | 3.333 | 3.99970 | 0.81% |
| 9.860E+09 | 25.355 | 0.3 | 5.000 | 3.99970 | 0.81% |
| 9.840E+09 | 25.407 | 0.4 | 6.667 | 4.01597 | 1.22% |
| 9.840E+09 | 25.407 | 0.5 | 8.333 | 4.01597 | 1.22% |
| 9.840E+09 | 25.407 | 0.6 | 10.000 | 4.01597 | 1.22% |
| 9.820E+09 | 25.458 | 0.7 | 11.667 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 0.8 | 13.333 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 0.9 | 15.000 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.0 | 16.667 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.1 | 18.333 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.2 | 20.000 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.3 | 21.667 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.4 | 23.333 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.5 | 25.000 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.6 | 26.667 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.7 | 28.333 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.8 | 30.000 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 1.9 | 31.667 | 4.03235 | 1.64% |
| 9.820E+09 | 25.458 | 2.0 | 33.333 | 4.03235 | 1.64% |

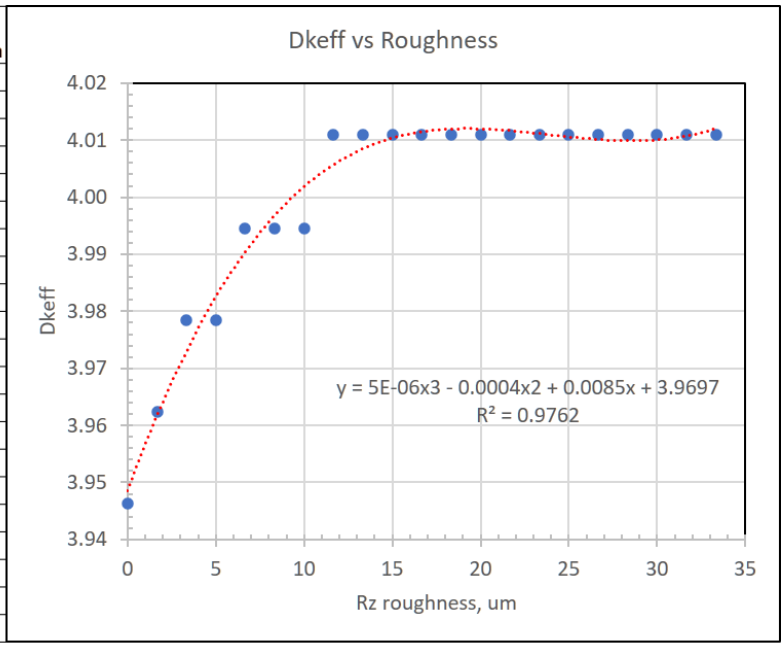


**Figure 11 Summary of extracted simulated results and graph plotting Dkeff vs Rz via conductor roughness**

### Dkeff due to pressed thickness

The Dkeff of individual cores and prepreg layers within the finished PCB varies based on their final pressed thickness. The actual core and prepreg thicknesses must be precisely measured from micro-sections of the tested board for accurate simulation correlation. Since stackups are typically designed using the published Dk/Df construction table values, these values differ from the actual pressed thickness after board fabrication. During the pressing process, under heat and pressure, the dielectric loses resin content. Because the published Dk is based on a specific resin content prior to pressing, the resin loss in the pressed dielectric results in an increase in Dk.

Figure 12 shows the relationship between bulk Dk and thickness for Tachyon 100G 1078 glass style. Since a change in thickness corresponds to a change in resin volume, a linear fit equation can be used to adjust Dk based on pressed thickness. Consequently, the respective Dk values must be adjusted accordingly before converting from Dkz to Dkxy.

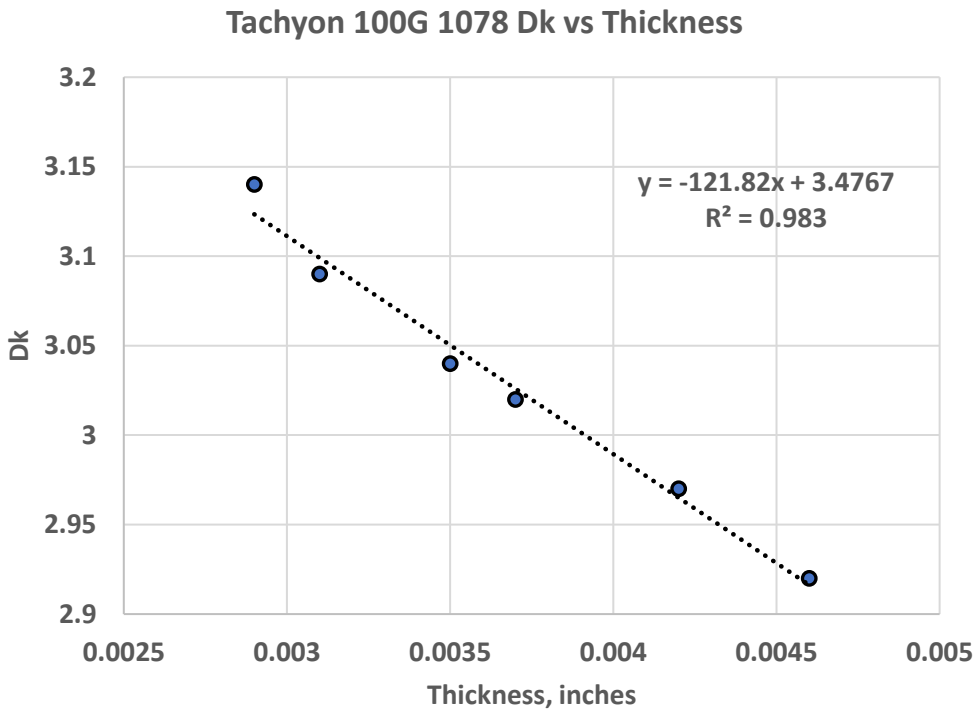


**Figure 12 Linear fit of Dk vs prepreg thickness for published values of Tachyon 100G 1078 glass style in [11].**

## Previous Study

In the DesignCon 2015 paper [5], the authors attempted to show that by using anisotropic dielectric models the modeling/simulation/measurement loop can be closed with simulation models of single-ended and differential vias. A simple test vehicle design was used to try and identify z-axis dielectric properties.

### Test Vehicle

A  picture of the test vehicle and stackup, taken from [5], are shown in Figure 13. The 12-layer PCB was fabricated with Tachyon 100G material.

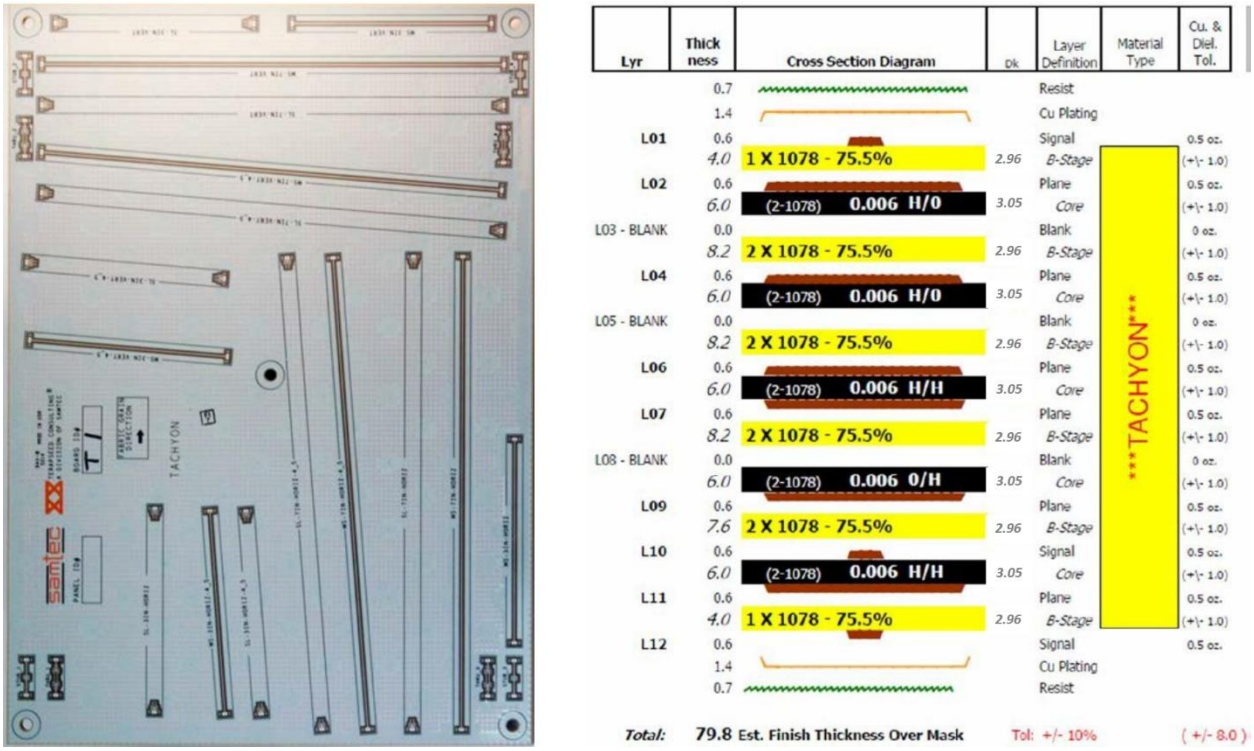


**Figure 13 Test vehicle PCB and stackup reference DesignCon 2015 paper [5].**

### Test Vehicle Model

The test vehicle HFSS simulation model is shown in Figure 14. A single microstrip trace, routed on the top layer, feeds a single via in the middle, creating a quarter-wave resonant structure. The via is surrounded by ground vias to localize the EM fields, approximating a coaxial structure as described earlier.

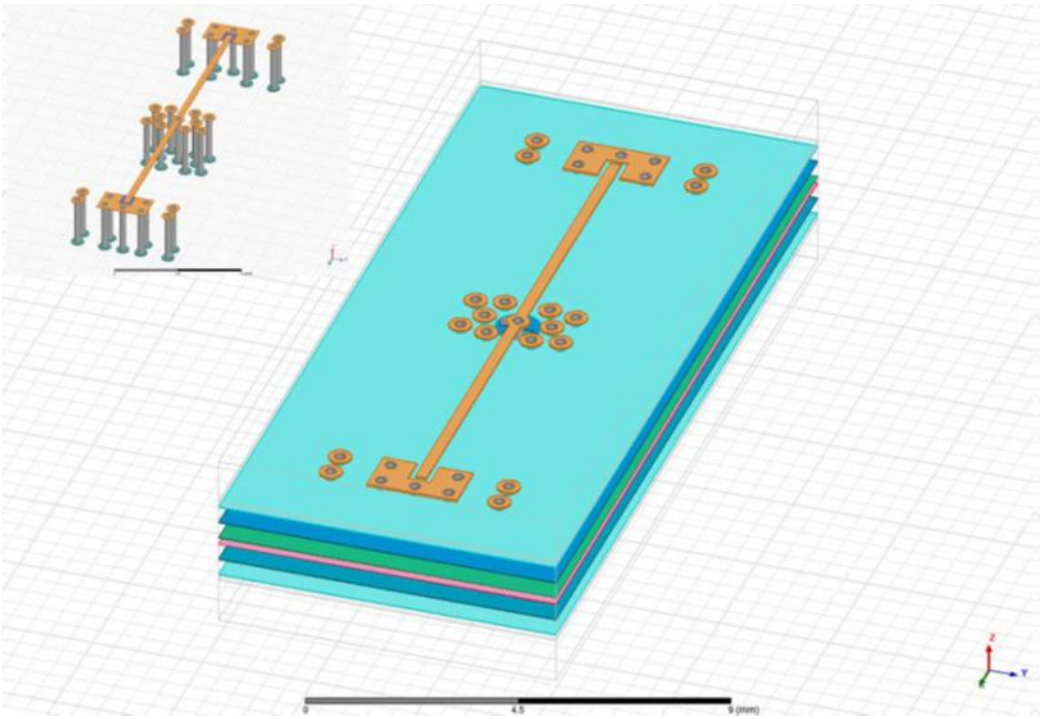

Figure 14 Simulation model used for analysis reference DesignCon 2015 paper [5].

**Anisotropy Test Vehicle Tachyon Results**

Unfortunately, final measurement and simulation results were unavailable by the time of the proceedings publication. To gather more data from this study, I reached out to my friend Scott McMorrow, who graciously shared additional as fabricated and simulation information [6].

Two via stub test structures, identified as Stub_1 and Stub_4, of the same design located at different locations on the same test vehicle panel were x-sectioned for analysis. Using measured parameters for both via lengths and the Dk values from the as-designed stackup, a difference in stub resonance frequency of 1.054% for Stub_1 and 1.057% for Stub_4 was observed. This difference corresponded to an as-fabricated effective anisotropy (Λeff) of 11% and 12%, respectively, based on empirical measurements.

## Extended Case Study

In the extended case study presented in this paper, I will use the as-fabricated cross-section measured parameters for Stub_1 to account for the discrepancy between the effective anisotropy and the heuristically derived anisotropy discussed in my DesignCon 2024 paper [1].

Figure 15 is the negative image from the original x-section photo of Stub_1 in [6]. The dielectric thickness measurements in yellow and summarized in the black box in the center of the via are from the original picture. After calibrating the microscope software to one of the original image dimensions, additional measurements for my case study were performed separately, with dimension lines shown in red.

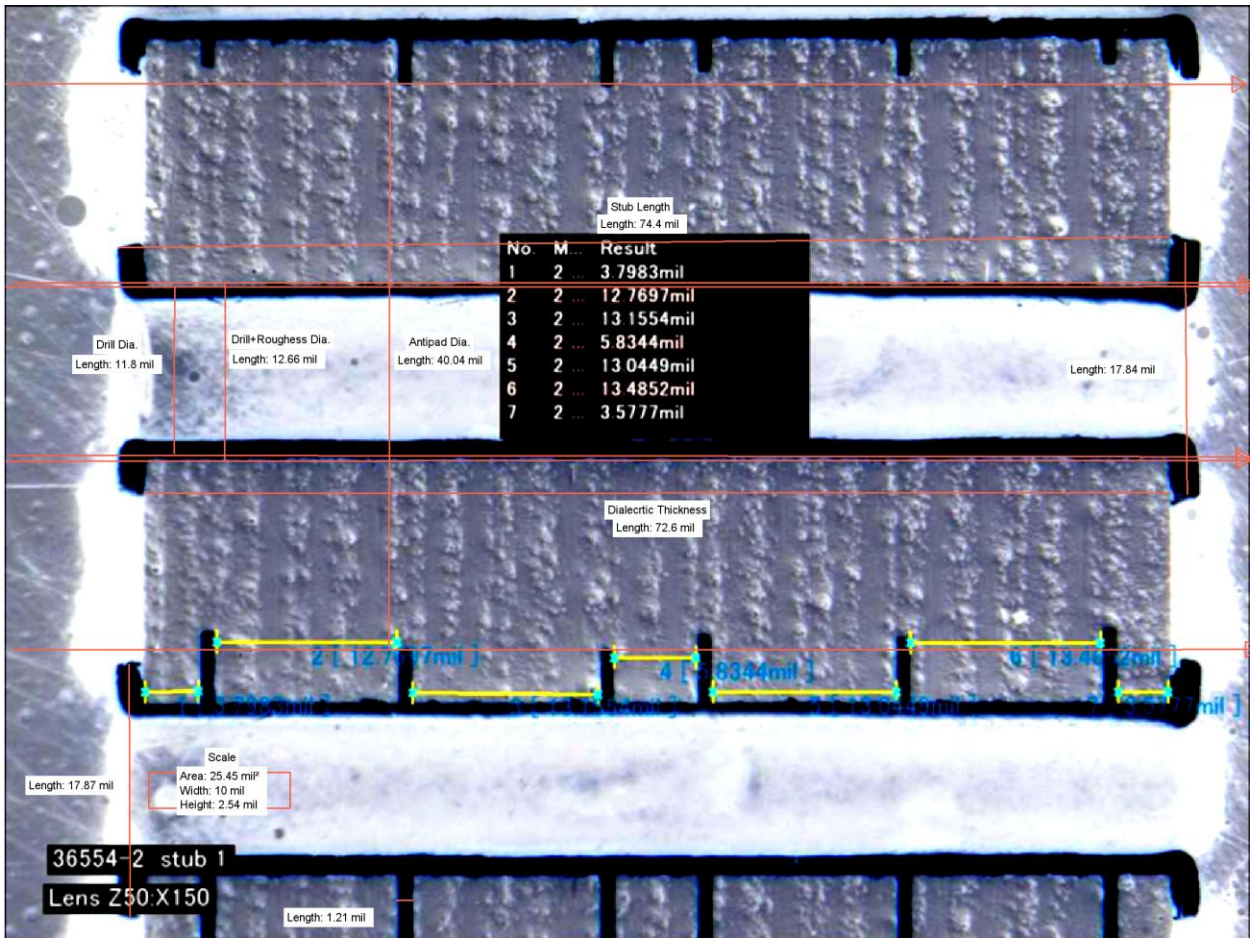


**Figure 15 Inverted image from original x-section photo of Stub_1 showing pressed dielectric thickness measurements in yellow. Additional measurements for this case study are shown in red. Original photo courtesy of Scott McMorrow [6]**

### Dkeff due to pressed thickness

Table 1 summarizes as-designed stackup parameters shown in Figure 13 vs the as-fabricated parameters and the effect on bulk Dk due to pressed thickness measured in Figure 15. To facilitate the comparison the individual core and prepreg thicknesses were combined or separated, as highlighted in yellow, to align with the equivalent x-section thickness measurements. In order to heuristically convert bulk Dkz to Dkxy single ply thickness is required and shown for completeness.

As we can see, the as-fabricated dielectric thickness is less than the as-designed thickness, resulting in an average bulk Dkz increase from 3.00 to 3.07, equivalent to 2.8%. Additionally, the average bulk Dkxy is 3.22, corresponding to an average anisotropy of 4.8%.

**Table 1 Summary of as-designed stackup parameters shown in Figure 11 vs the as-fabricated parameters and the effect on bulk Dk due to pressed thickness measured in Figure 13.**

| No. | M | | Stackup mil | Stackup mil | As Designed Dkz Stackup | X-sec Meas Thick mil | X-sec Stackup mil | Pressed Single ply thickness mils | Pressed Dkz X-sec (linear fit) | Pressed Dkxy Calculated | Pressed Anisotropy |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | Bstage | | 4 | 2.96 | 3.80 | 3.80 | 3.80 | 3.01 | 3.14 | 4.2% |
| | | | | | | | | | | | |
| 2 | 2 | core | | 6 | 3.05 | 12.77 | 5.8344 | 2.92 | 3.12 | 3.28 | 5.1% |
| | | Bstage | 14.2 | 8.2 | 2.96 | | 6.9353 | 3.47 | 3.05 | 3.2 | 4.8% |
| | | | | | | | | | | | |
| 3 | 2 | core | | 6 | 3.05 | 13.16 | 5.8344 | 2.92 | 3.12 | 3.28 | 5.1% |
| | | Bstage | 14.2 | 8.2 | 2.96 | | 7.321 | 3.66 | 3.03 | 3.17 | 4.6% |
| | | | | | | | | | | | |
| 4 | 2 | Core | | 6 | 3.05 | 5.83 | 5.8344 | 2.92 | 3.12 | 3.28 | 5.1% |
| | | | | | | | | | | | |
| 5 | 2 | Bstage | | 8.2 | 2.96 | 13.04 | 7.2105 | 3.61 | 3.04 | 3.18 | 4.7% |
| | | Core | 14.2 | 6 | 3.05 | | 5.8344 | 2.92 | 3.12 | 3.28 | 5.1% |
| | | | | | | | | | | | |
| 6 | 2 | Bstage | | 7.6 | 2.96 | 13.49 | 7.6508 | 3.83 | 3.01 | 3.14 | 4.3% |
| | | Core | 13.6 | 6 | 3.05 | | 5.8344 | 2.92 | 3.12 | 3.28 | 5.1% |
| | | | | | | | | | | | |
| 7 | 2 | Bstage | | 4 | 2.96 | 3.58 | 3.58 | 3.58 | 3.04 | 3.18 | 4.6% |
| | | | | | | | | | | | |
| **Averages** | | | | | **3.00** | | | | **3.07** | **3.22** | **4.8%** |

**Dielectric Dkeff Compensation Due to Conductor Roughness**

From the x-section measurements shown in Figure 15, Drillϕsmooth = 11.80 mils (299.7 µm); Drillϕrough = 12.66 mils (321.6 µm) and Antipadϕ = 40.04 mils (1.017 mm); and Dkeffsmooth = 3.22 from Table 1, using Equation 5 the effective Dkxy due to roughness (Dkeffxyrough) is calculated to be;

**Equation 9**

$$Dkeffxy_{rough} \cong \frac{\ln\left(\frac{40.04}{11.80}\right)}{\ln\left(\frac{40.04}{12.66}\right)} \times 3.22$$
$$\cong 1.06 \times 3.22 \cong 3.42$$

which increases Dkeffxy by 6.2%.

Not counting for Dkeff correction due to inductance caused by roughness, the modeled anisotropy of the as-fabricated via Stub_1 is:

**Equation 10**

$$\Lambda eff_{rough} \cong \frac{Dkeffxy_{rough}}{Dkeffz_{pressed}} - 1 \cong \frac{3.42}{3.07} - 1$$
$$\cong 0.114 \text{ or } 11.4\%$$

Taking the difference between Drillϕrough and Drillϕsmooth and dividing by 2, the surface roughness of the via barrel is approximately 0.43 mils (10.9 µm). Without modeling the actual via used in this case study, and assuming the contribution to Dkeff due to added inductance caused by roughness is roughly the same as the example in Figure 9, the polynomial fit equation from Figure 11 suggests that a 10.9 µm roughness adds another 1.36%.

This brings the total effective anisotropy to:

**Equation 11**

$$\Lambda eff_{total} \cong 11.4\% + 1.4\%$$
$$\cong 12.8\%$$

resulting in a final Dkeff of:

**Equation 12**

$$Dkeff_{final} \cong 3.22 \times 1.12$$
$$\cong 3.61$$

Figure 16, is a comparison of simulated and measured insertion loss results, taken from the presentation in [6]. Using measured parameters for stub lengths and the Dk values from the as-designed stackup in the HFSS model the simulated quarter-wave resonant frequency is approximately 22.1GHz, while the measured frequency was approximately 21 GHz.

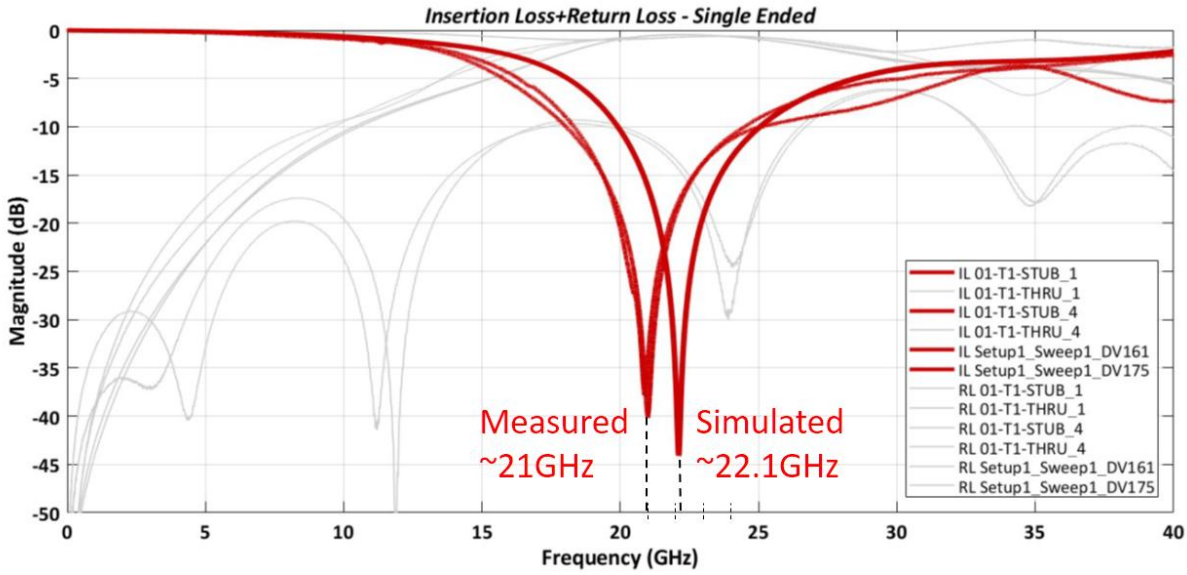


**Figure 16 Measured vs simulated insertion loss results taken from reference [6]**

Using a stub length (StubLen) of 74.4 mils (1.89 mm) from x-section Figure 15 and applying Equation 13 & Equation 14 below, Dkeffmeas is 3.60 and Dkeffsim is 3.21 for an Λeff of 12.15%.

**Equation 13**

$$Dkeff_{meas} = \left(\frac{c}{4 \times fo \times StubLen}\right)^2$$
$$= \left(\frac{1.18E10}{4 \times 21.0E9 \times 74.4E-3}\right)^2$$
$$\cong 3.6$$

**Equation 14**

$$Dkeff_{sim} = \left(\frac{c}{4 \times fo \times StubLen}\right)^2$$
$$= \left(\frac{1.18E10}{4 \times 22.1E9 \times 74.4E-3}\right)^2$$
$$\cong 3.2$$

**Equation 15**

$$\Lambda_{eff} = \frac{3.6}{3.2} - 1 = 12.5\%$$

The comparison between the effective anisotropy calculated in Equation 11 (12.8%) and the effective anisotropy measured in Equation 15 (12.5%), along with the comparison of the final calculated Dkeff

from Equation 12 (3.61) to the measured Dkeff from Equation 13 (3.60), demonstrates excellent correlation at 21 GHz, thereby validating my hypothesis.

## Summary and Conclusions

This paper has explained why material anisotropy is not solely responsible for contributing to Dkeff surrounding a via hole structure. The via barrel conductor roughness and resin content of the as fabricated dielectric pressed thicknesses must be considered and adjusted before applying my heuristic method to calculate Dkxy.

The extended case study from [6] revealed an effective anisotropy of 12.5% compared to bulk material anisotropy of 4.8 % predicted by my heuristic method [1]. Based on cross-section data from the extended case study, adjusting Dkeff for pressed thickness and via roughness adds an additional 8% to the effective anisotropy thereby validating my hypothesis.

## Acknowledgements

I would like to thank Juliano Mologni from Ansys for his help with via simulations and Scott McMorrow from Samtec for providing additional as fabricated and simulation data from his DesignCon 2015 paper follow-up case study. I also like to thank Dr. Alexandre Gutterman for reviewing and providing feedback to improve clarity.

## Reference:

[1] Bert Simonovich, “A Heuristic Approach to Assess Anisotropic Properties of Glass-reinforced PCB Substrates”, DesignCon 2024 proceedings, Santa Clara, CA.
[2] Bert Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness", DesignCon 2017 proceedings, Santa Clara, CA.
[3] Bert Simonovich, “A Tale of Two Data Sheets and How Foil Roughness Affects Dk”, White Paper, Lamsim Enterprises Inc., Issue 03, March 7, 2022.
[4] IPC-600G, “Acceptability of Printed Boards”, July 2004.
[5] Scott McMorrow et al, “Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions”, DesignCon 2015 proceedings, Santa Clara, CA.
[6] Scott McMorrow, “Anisotropy Test Vehicle Tachyon Results”, Samtec presentation, 2022.
[7] Al Neves et al, “Free Signal Integrity? How Understanding Anisotropic Materials & Tolerances Could Increase Performance at 112/224Gbps & Beyond”, DesignCon 2025 proceedings, Santa Clara, CA.
[8] J.E. Bracken, “A Causal Huray Model for Surface Roughness.”, DesignCon 2012 proceedings, Santa Clara, CA.
[9] Bert Simonovich, “Practical Method for Modeling Conductor Surface Roughness Using The Cannonball Stack Principle”, White Paper, Issue 2, April 25, 2015
[10] Ansys HFSS, [computer software].
[11] Isola Tachyon 100G Dk/Df construction table.
[12] Keysight Pathwave Advanced Design System (ADS) [computer software], (Version 2025 update2).